

# Compal Confidential

## QCL51 Schematics Document

### AMD Comal Platform

### AMD Trinity APU / Hudson FCH / ATI Chelsea Pro M2

### Muxless/UMA / PX 4.0 / PX 5.0

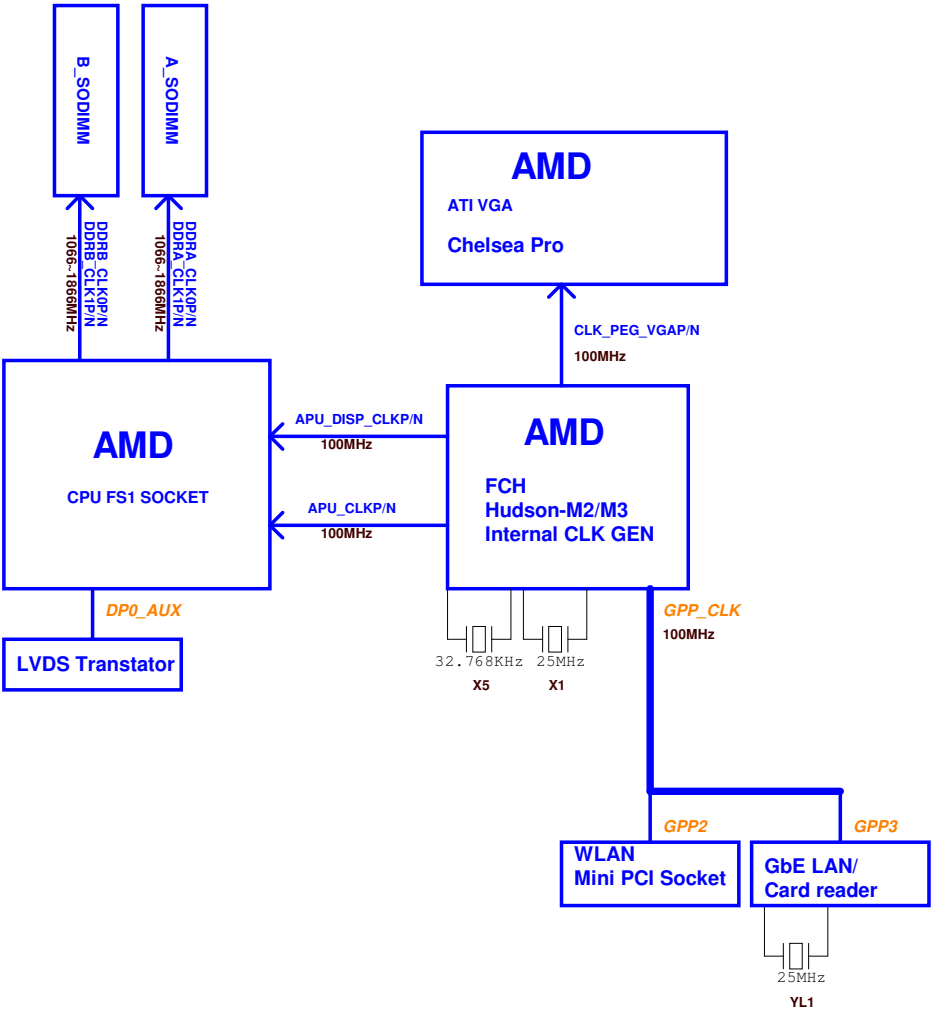
2011-10-26

LA-8712P REV: 0.1

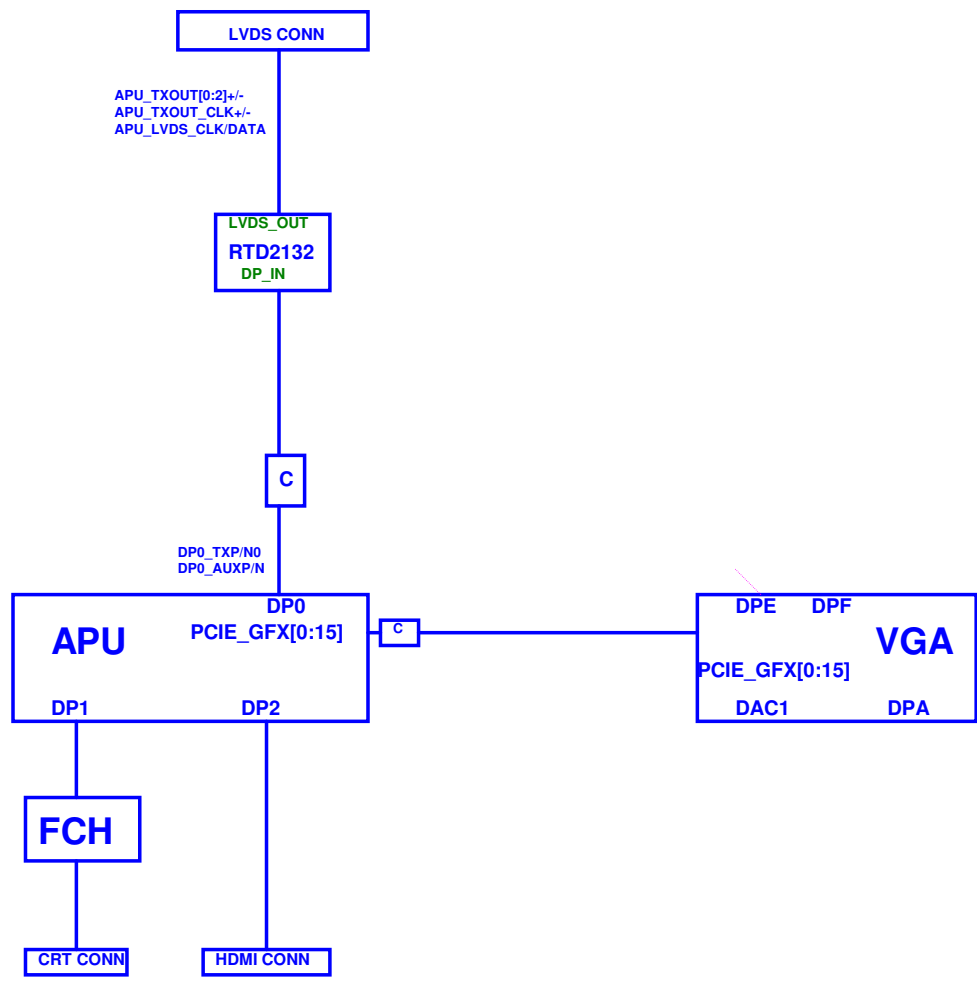
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Issued Date	2011/07/08	Deciphered Date	2015/07/08	Title	Cover Page
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Issued Date	2011/07/08	Deciphered Date	2015/07/08	Title	Block Diagrams
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CLOCK DISTRIBUTION



DISPLAY OUTPUT



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Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+APU_CORE	Core voltage for CPU	ON	OFF	OFF
+APU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+VDDCI	0.95-1.2V switched power rail	ON	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	ON	OFF
+0.935VGS	0.935V switched power rail for VGA	ON	OFF	OFF
+1.1ALW	1.1V switched power rail for FCH	ON	ON	ON*
+1.1VS	1.1V switched power rail for FCH	ON	OFF	OFF
+1.2VS	1.2V switched power rail for APU	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.5V_PCIE	1.5V switched power rail	ON	OFF	OFF
+1.8VGS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+LAN_VDD_3V3	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE	SIGNAL							
	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rb	100K +/- 5%			
Board ID	Ra / Rb	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V



PCB  
Part Number = DA80000SH00  
PCB 00H LA-8712P REV0 M/B

BOARD ID Table

Board ID	PCB Revision
0	DB
1	
2	
3	
4	
5	
6	
7	

BOM Option Table

BOM  
Structure  
PX@

Description  
UMA  
PX function

BOM Config

PX  
V

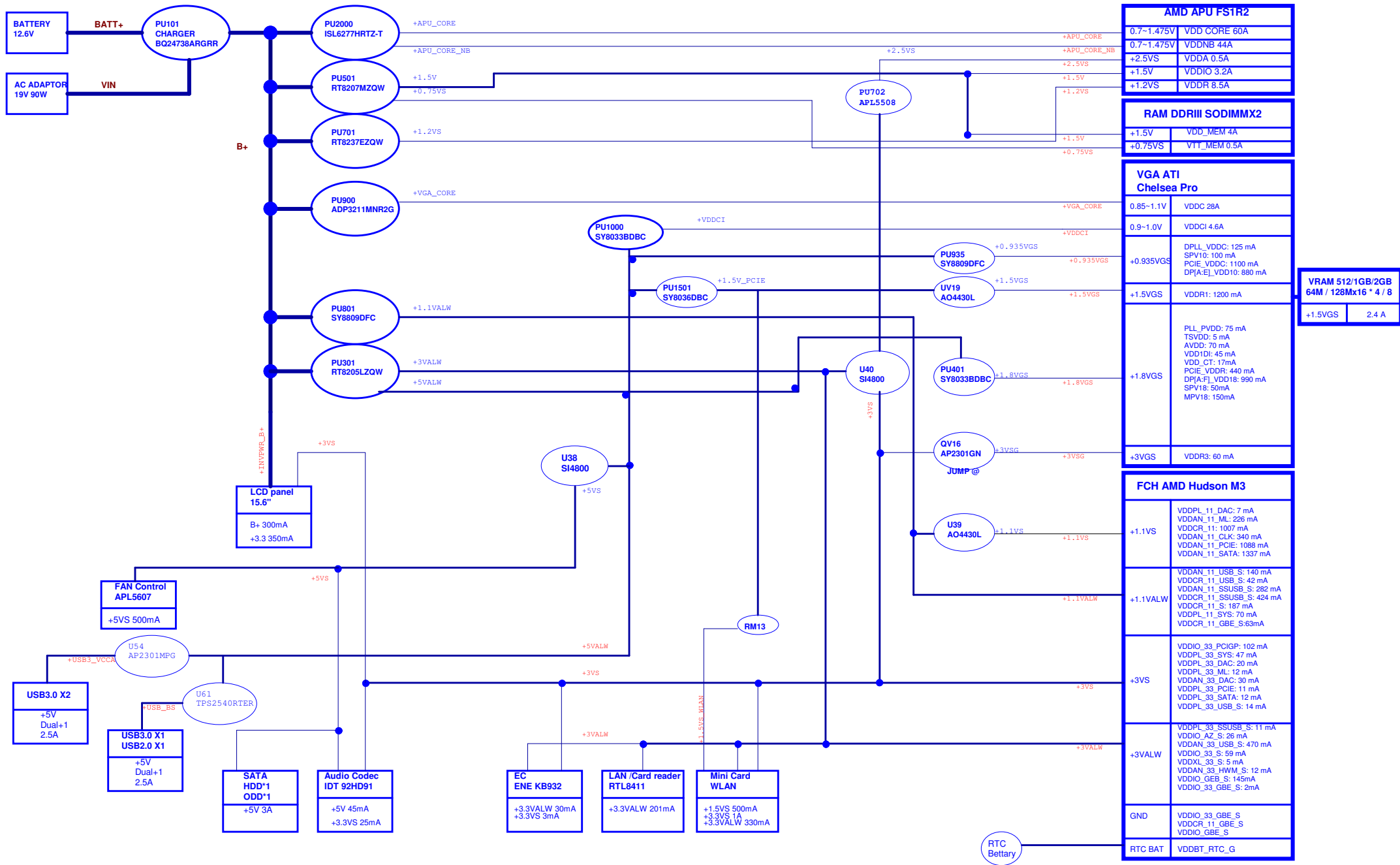
x = 1 is read cmd, x= 0 is write cmd.

External PCI Devices			
Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address			EC SM Bus2 address		
Device	Address	HEX	Device	Address	HEX
Smart Battery	0001 011X b	16H	ADI ADM1032 (GPU)	1001 101X b	9AH
			SB-TSI (APU)	1001 100X b	98H
			LVDS TR	1010 100X b	A8H
			VGA Internal Thermal	1000 001X b	82H

FCH (S0) SM Bus 0 address			FCH (S0~S5) SM Bus 1 address		
Device	Address	HEX	Device	Address	HEX
DDR DIMM1	1010 000X b	A0	Touch pad		
DDR DIMM2	1010 001X b	A2			
Amplifier					

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13 PCIE\_GTX\_C\_FRX\_P[0..15]

13 PCIE\_GTX\_C\_FRX\_N[0..15]

PCIE\_FTX\_C\_GRX\_P[0..15] 13

PCIE\_FTX\_C\_GRX\_N[0..15] 13

GPU

GLAN/Card reader  
WLAN

UMI

GPU

GLAN/Card reader  
WLAN

UMI

JCPU1A

PCI EXPRESS

GRAPHICS

GPP

UMI

+1.2VS R539 196\_0402\_1% P\_ZVDDP AG11

P\_ZVDDP W/S=8/12 mil, &lt;3000mil

LOTES\_ACA-ZIF-109-P12-A\_FS1R2  
CONN@

P\_ZVSS

AH11 P\_ZVSS R540 196\_0402\_1%

P\_ZVSS W/S=8/12 mil, &lt;3000mil

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Title

AMD FS1R2 PCIE / GFX / UMI

Size

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Monday, November 28, 2011

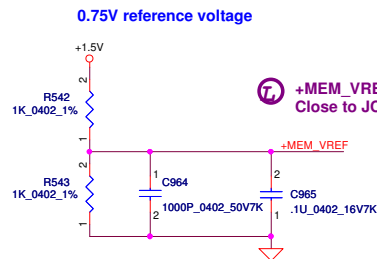
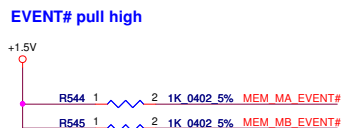
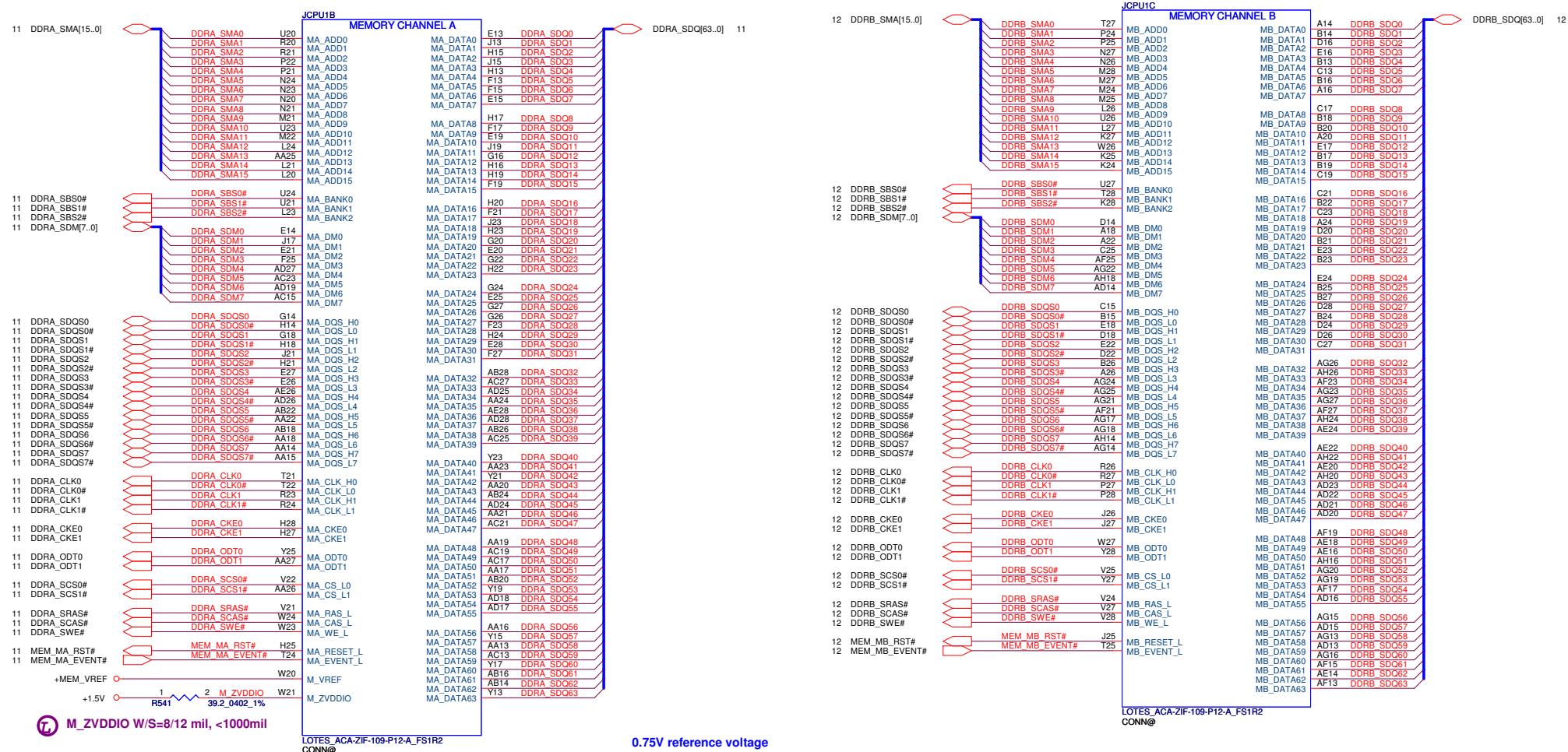
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Issued Date	2011/07/08	Deciphered Date	2015/07/08	AMD FS1 DDRIII I/F	
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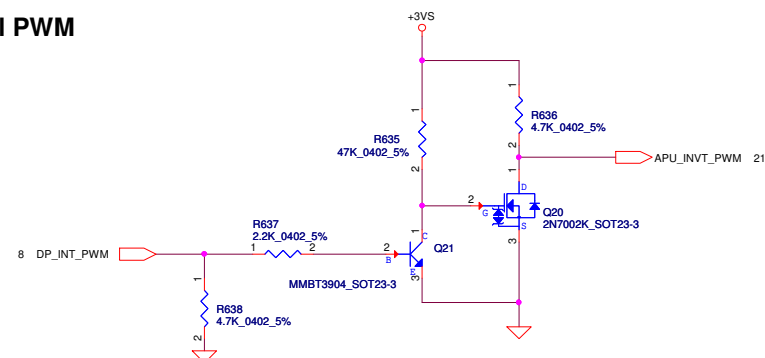
**LA-8124 no use this DP\_ENBKL.**



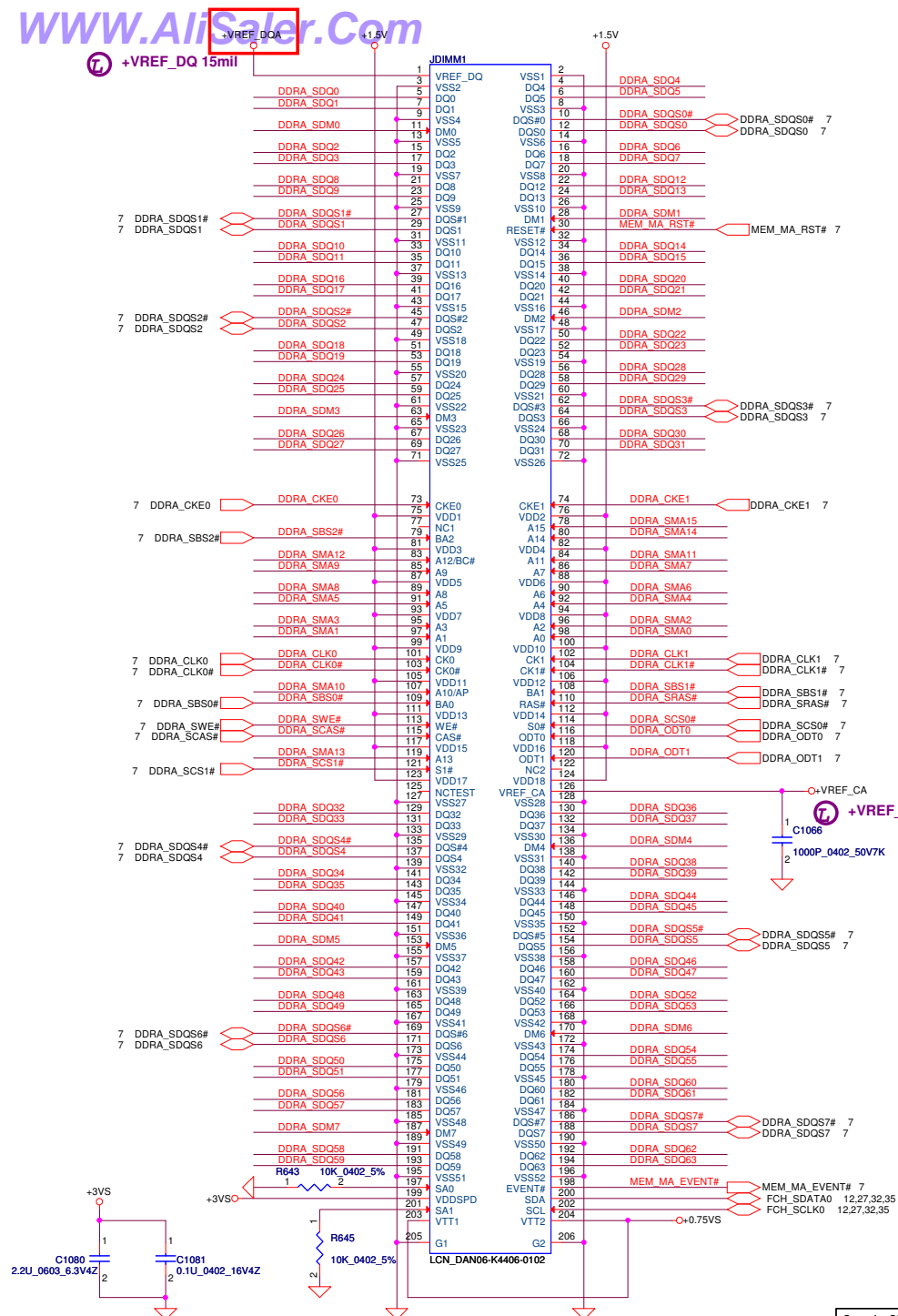
## eDP Panel ENVDD



### Panel PWM

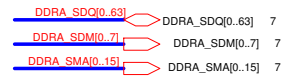


Security Classification	Compal Secret Data			Title	AMD FS1R2 Singal Level Shifter	Rev	0.1
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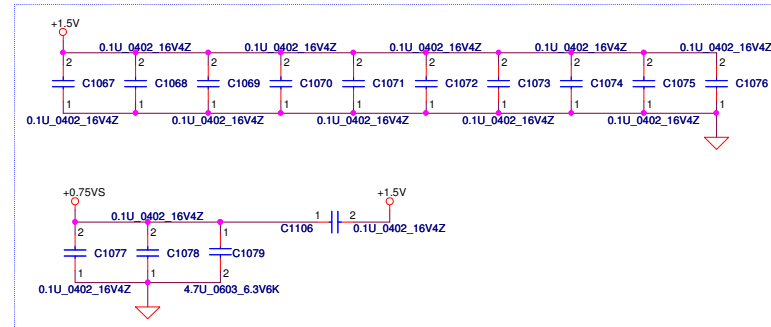


# DIMM\_A REV H:4mm

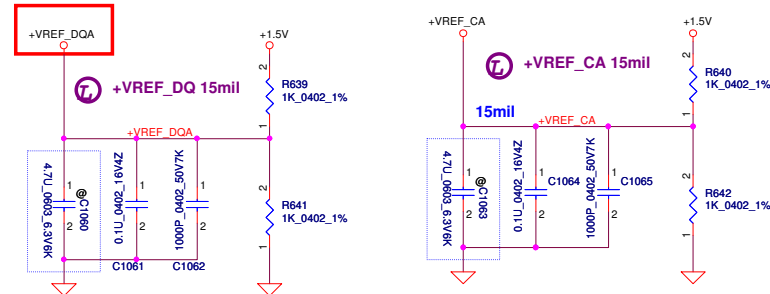
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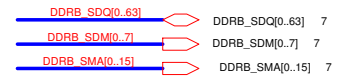
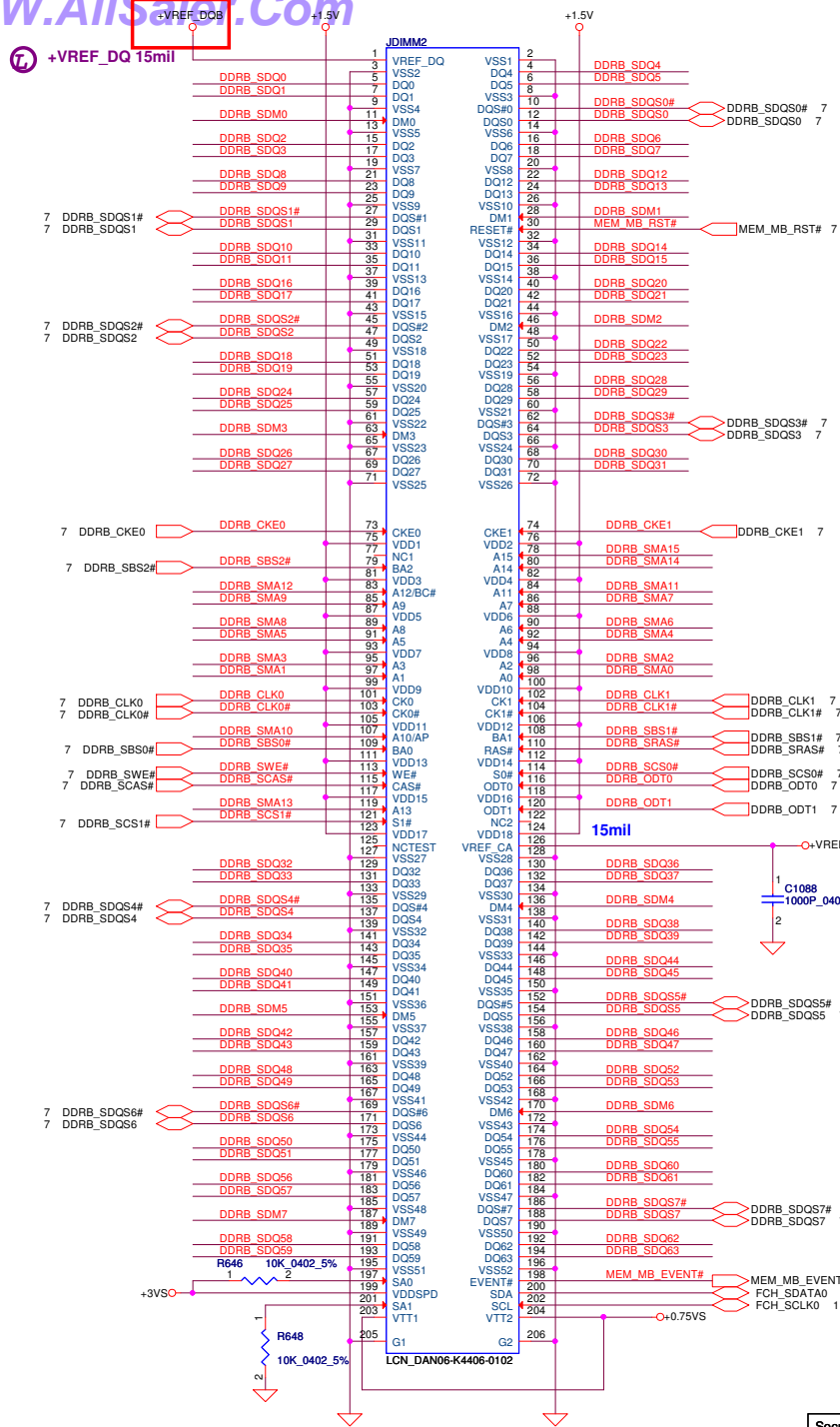
## Place near DIMM1



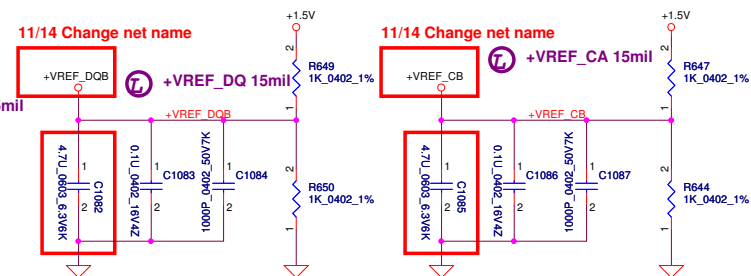
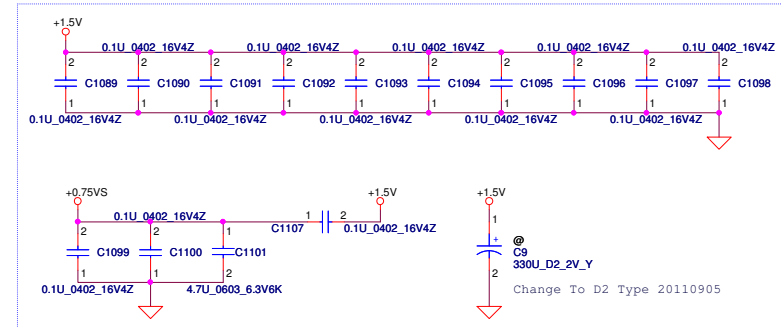
## 11/14 Change net name



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**Place near DIMM2**



**DIMM B REV H:8mm**

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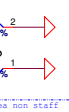
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**Update net nam**

Component	Value	Pin	GPIO Pin
10K	0402 5%	1	GPIO24 TRSTB
2	RV18	2	GPIO25 TDI
10K	0402 5%	1	GPIO27 TMS
2	RV19	2	GPIO26 TCK
10K	0402 5%	1	-
2	RV20	2	-
10K	0402 5%	1	-
2	RV21	2	-

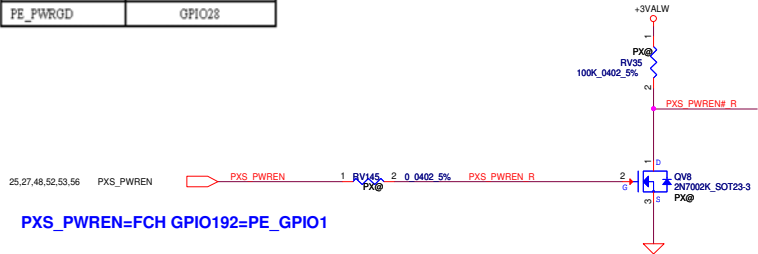


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EXCEPT A  
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Name	FCH Pin Assignments
	Hudson-2/Hudson-3
PE_GPIO0	GPIO191
PE_GPIO1	GPIO192
PE_PWRGD	GPIO28

GPU\_Reset  
PWREN

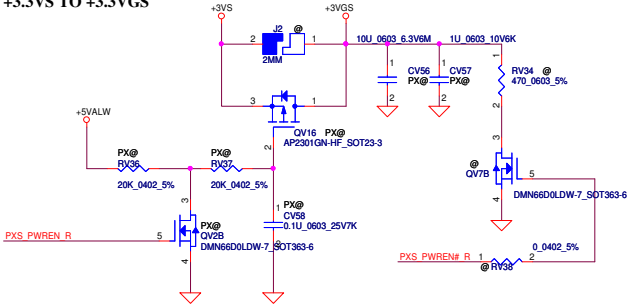


Del +1.8VGS DC DC



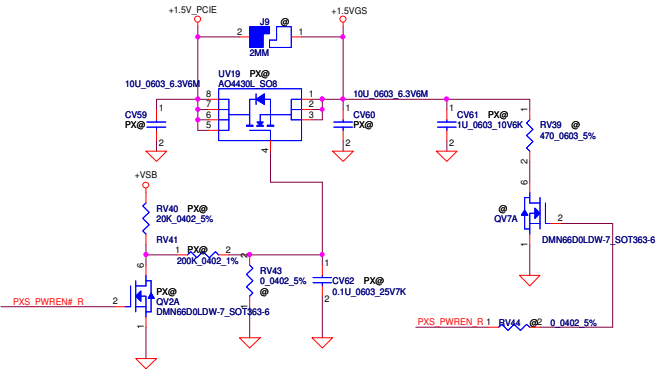
11/10 follow Lotus

+3.3VS TO +3.3VGS

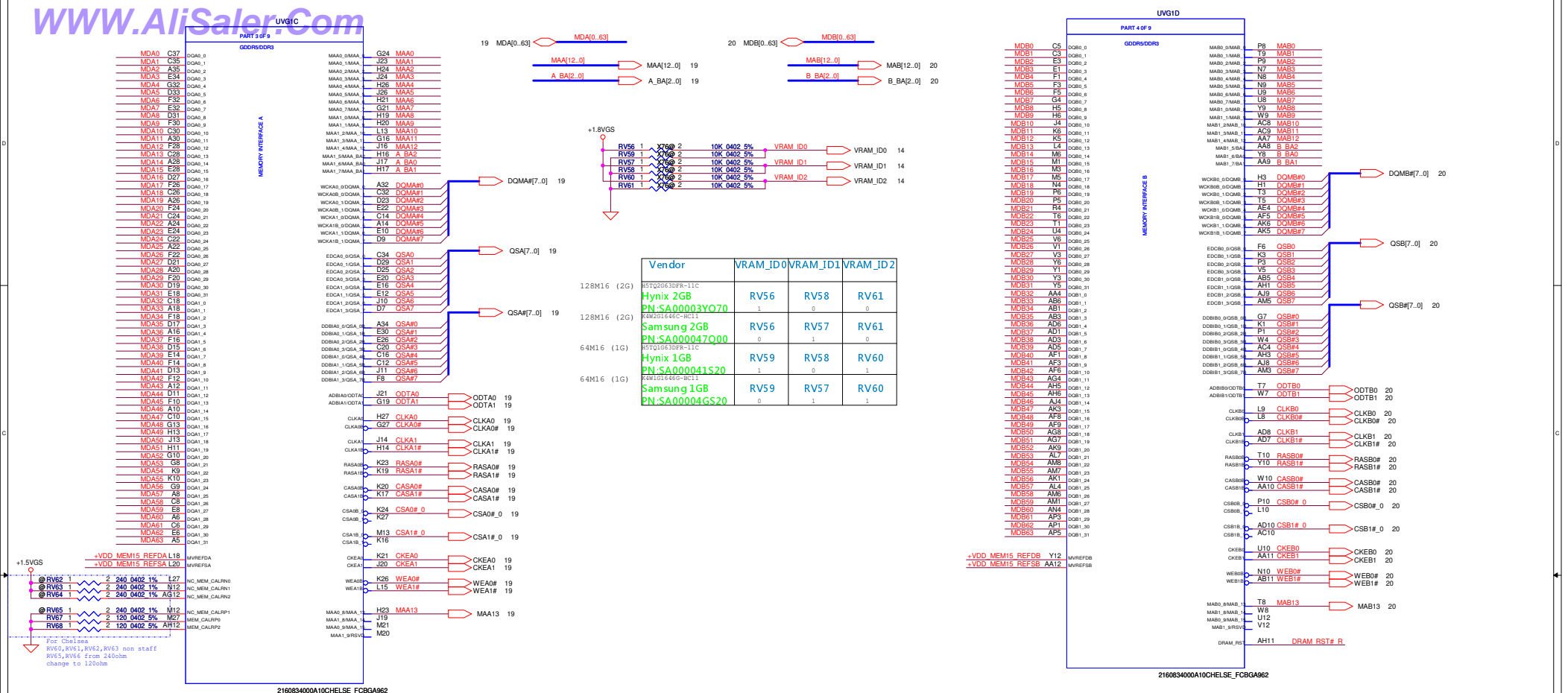


+1.5V\_PCIE TO +1.5VGS

Add +1.5VGS DC DC

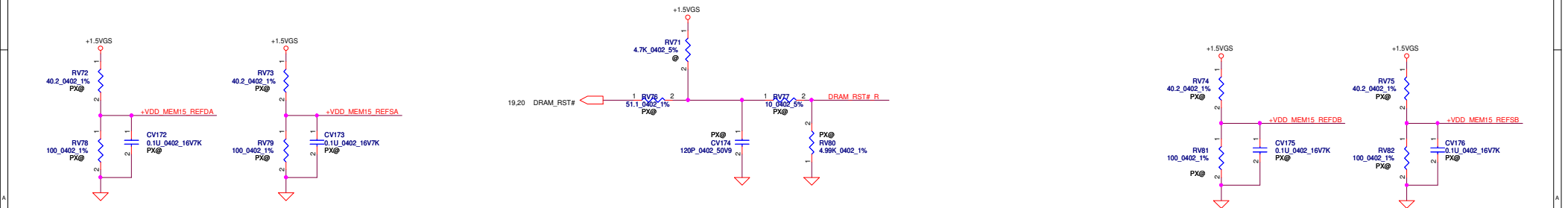


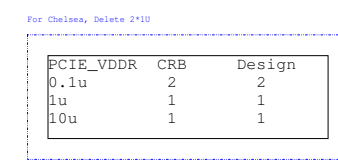




This basic topology should be used for DRAM\_RST for DDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM load and board to pass Reset Signal Spec.

Place all these components very close to GPU (Within 25mm) and keep all component close to each other (within 5mm) except Rser2





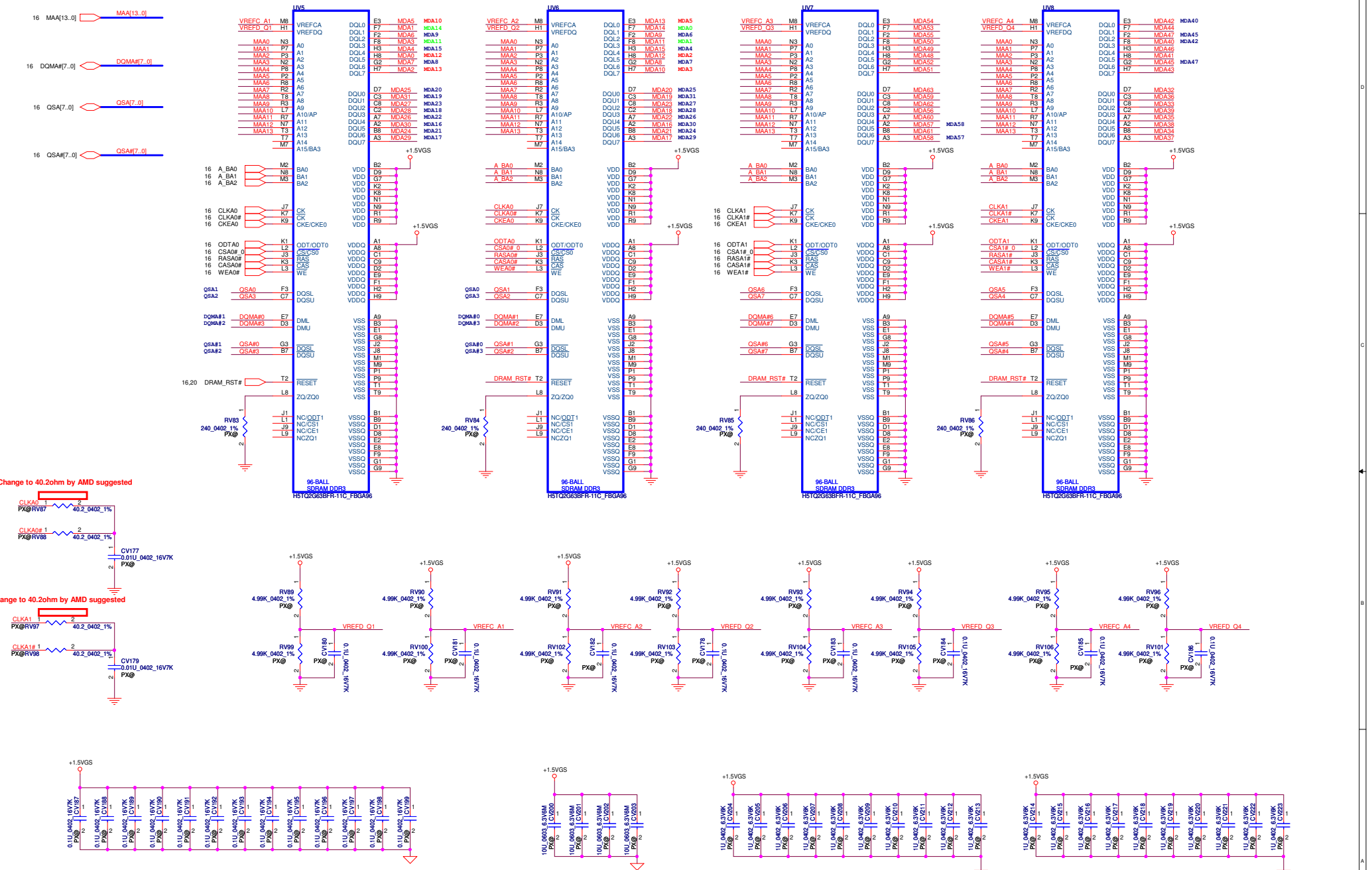
PCIE_VDDC	CRB	Design
1u	7	5 (1@)
10u	1	1

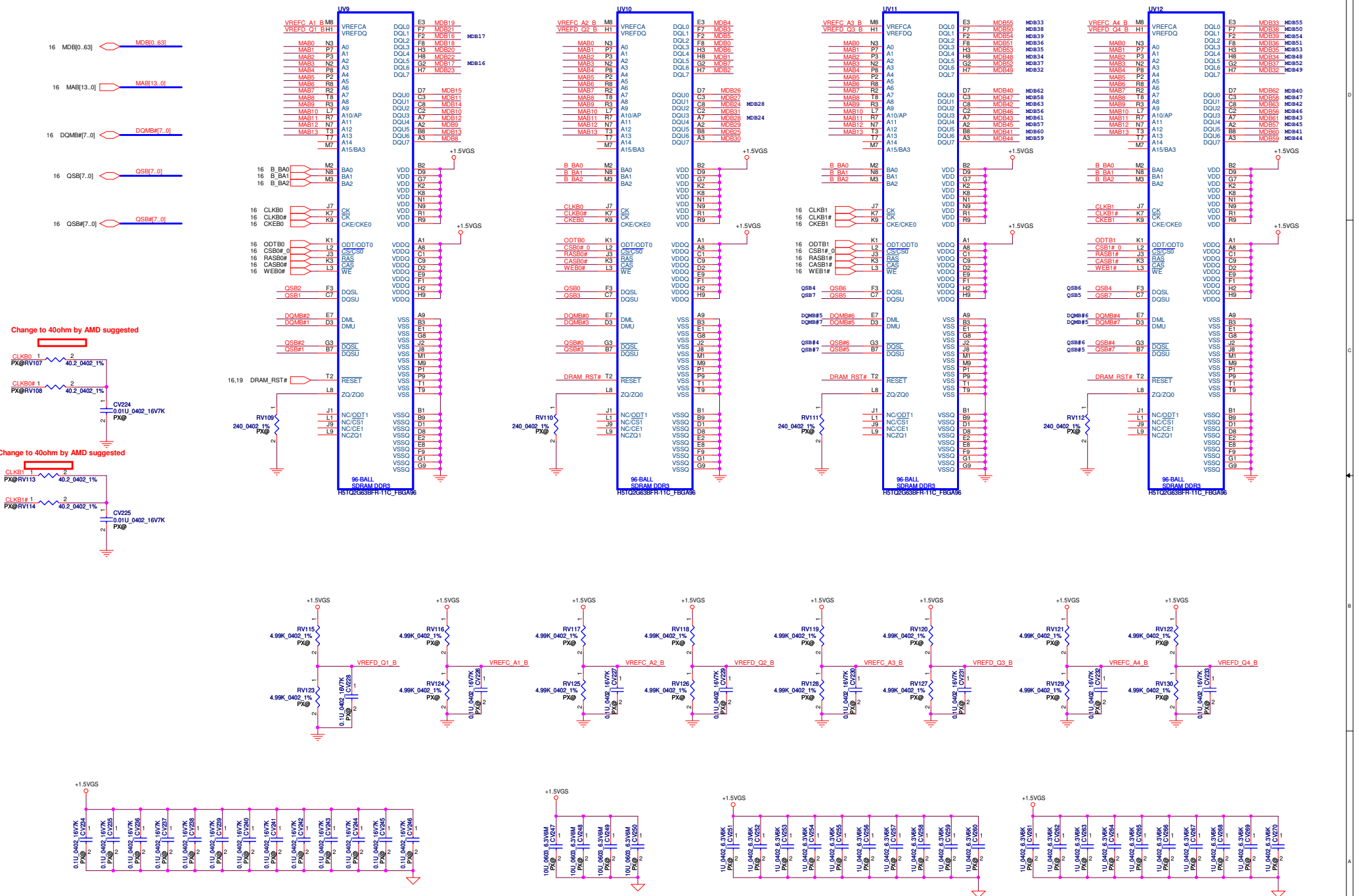
VDDC	CRB	Design
1u	30	25
10u	10	1
22u	0	1

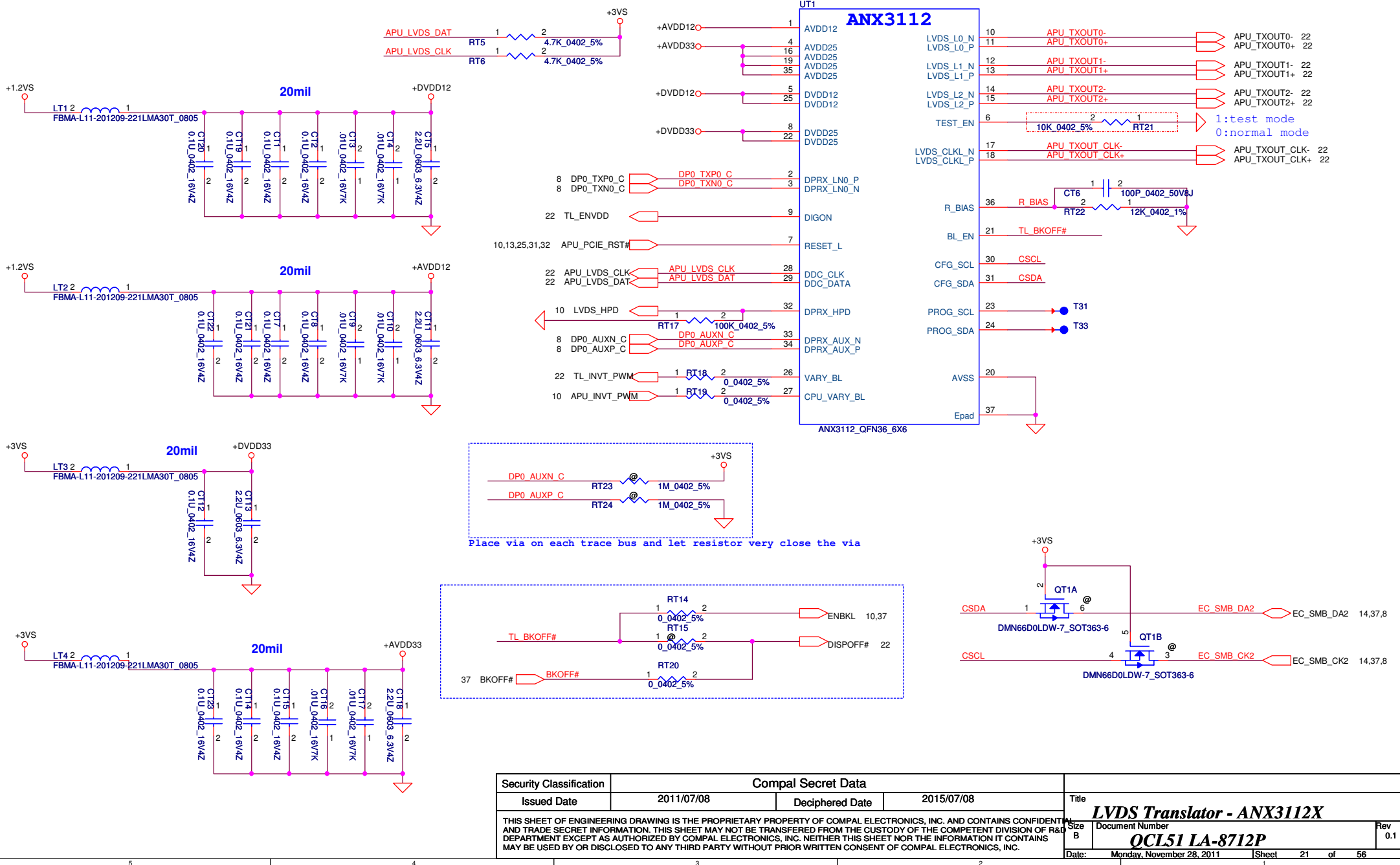
VDDCI	CRB	Design
1u	10	9
10u	3	2
22u	0	1

**VDDCI and VDDC should have separate regulators with a merge option on PCB**  
**For Madison, Park, Capilano, Robson, Seymour and Whistler, VDDCI and VDDC can share one common regulator**

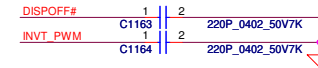
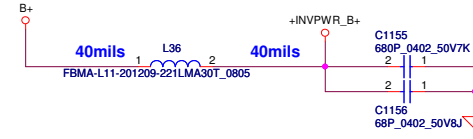
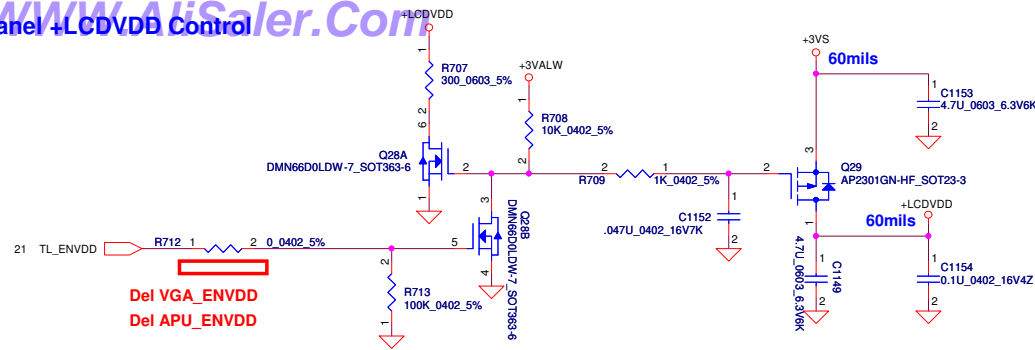






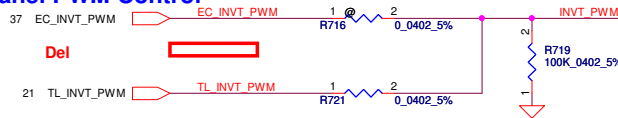


### Panel +LCDVDD Control

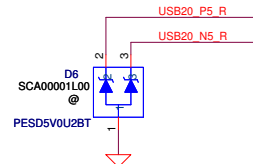
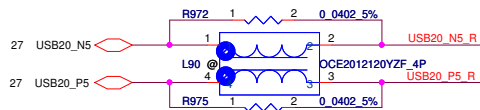


## Panel Backlight Control

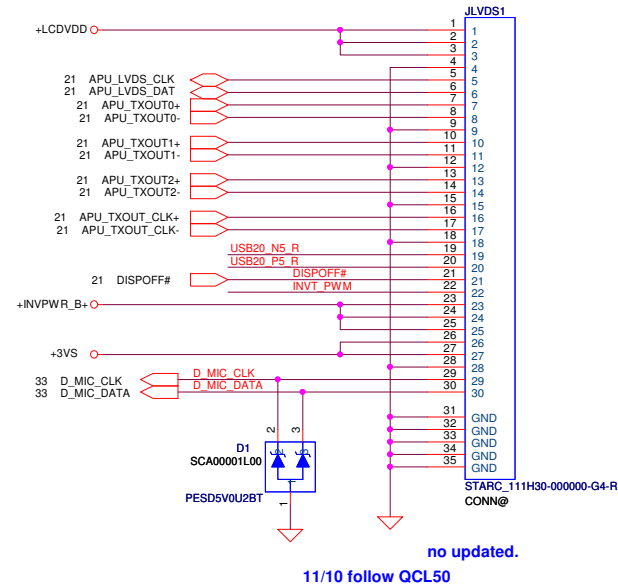
**Modify and change to page 21**



<Translator LVDS Output>



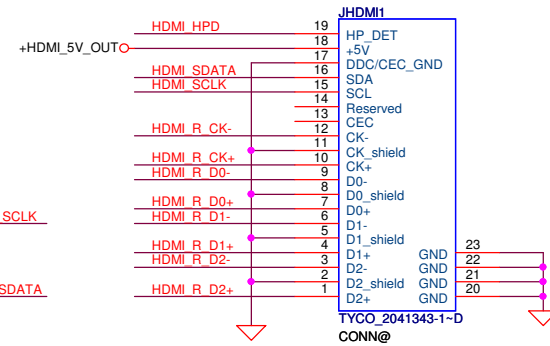
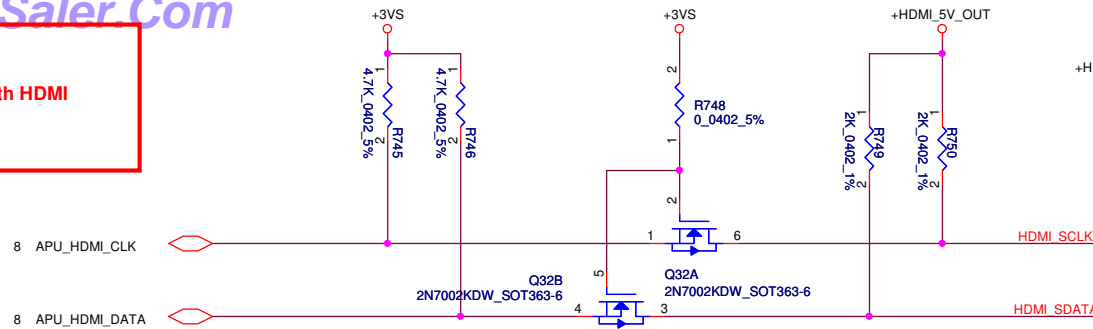
## LVDS Connector



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Combine with HDMI

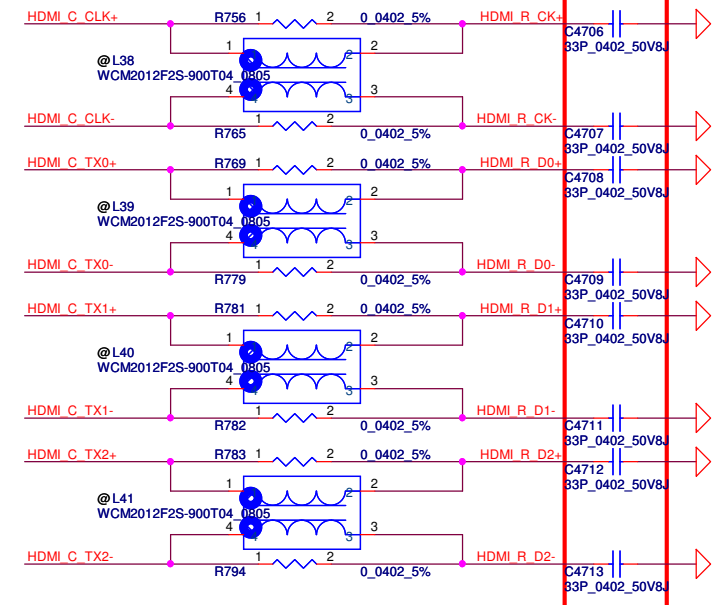
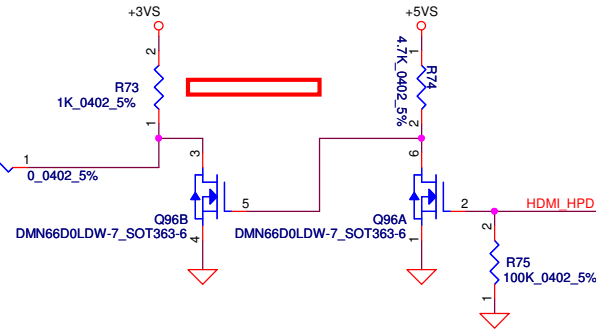


11/05 update footprint.

Del VGA\_HDMI\_DET



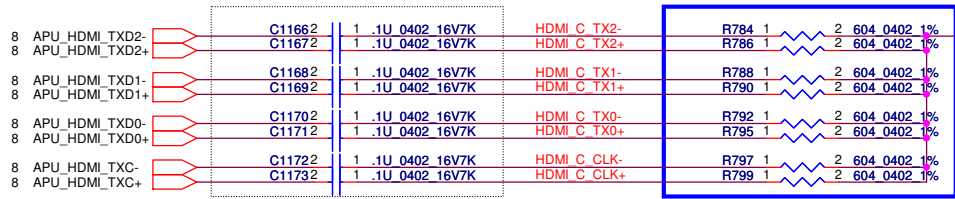
8 DP2\_HPD  
For APU\_HDMI\_HPD



11/15 EMI  
Near connector

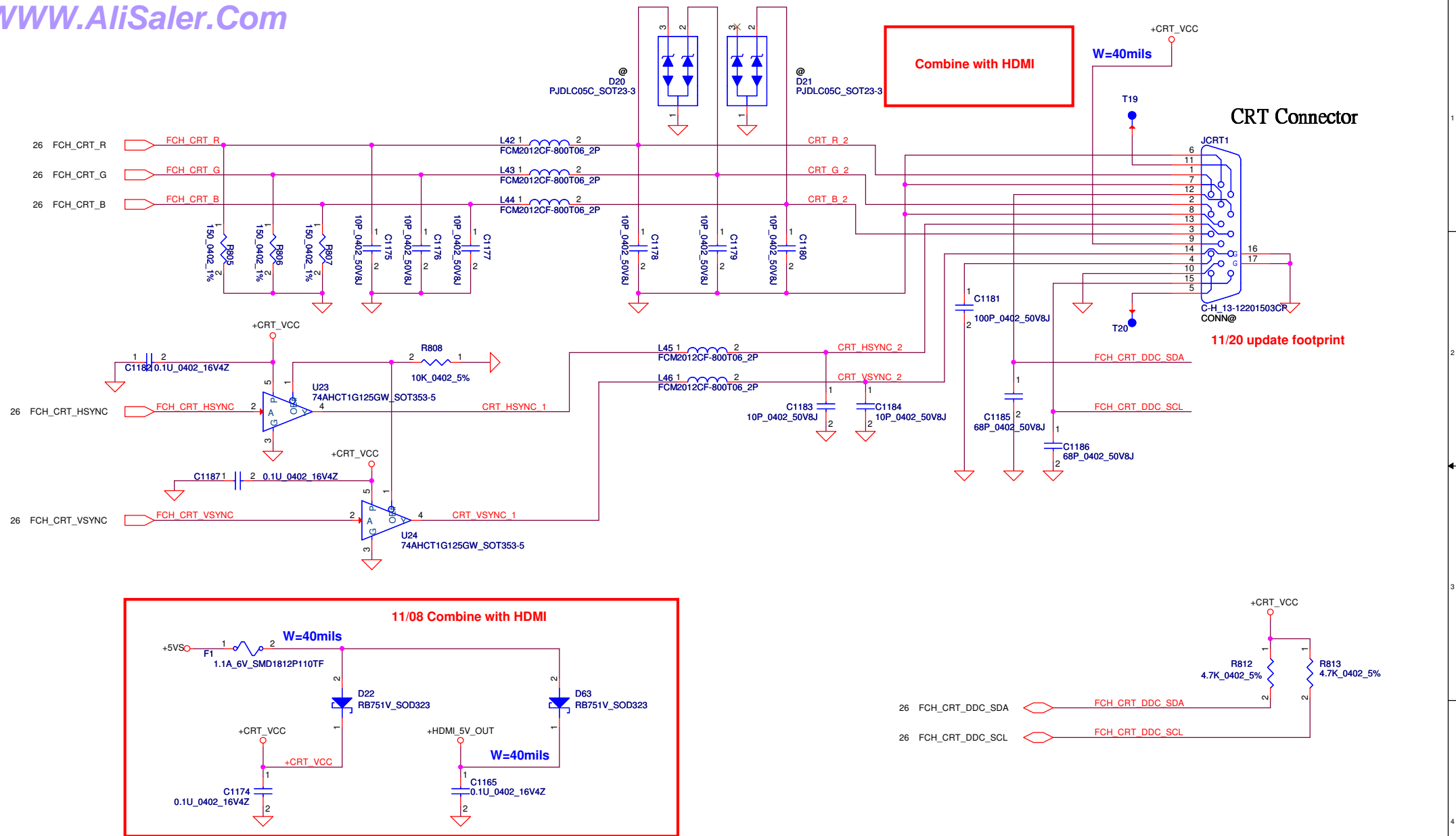
Close to HDMI conn

10/27 change to 604 ohm.

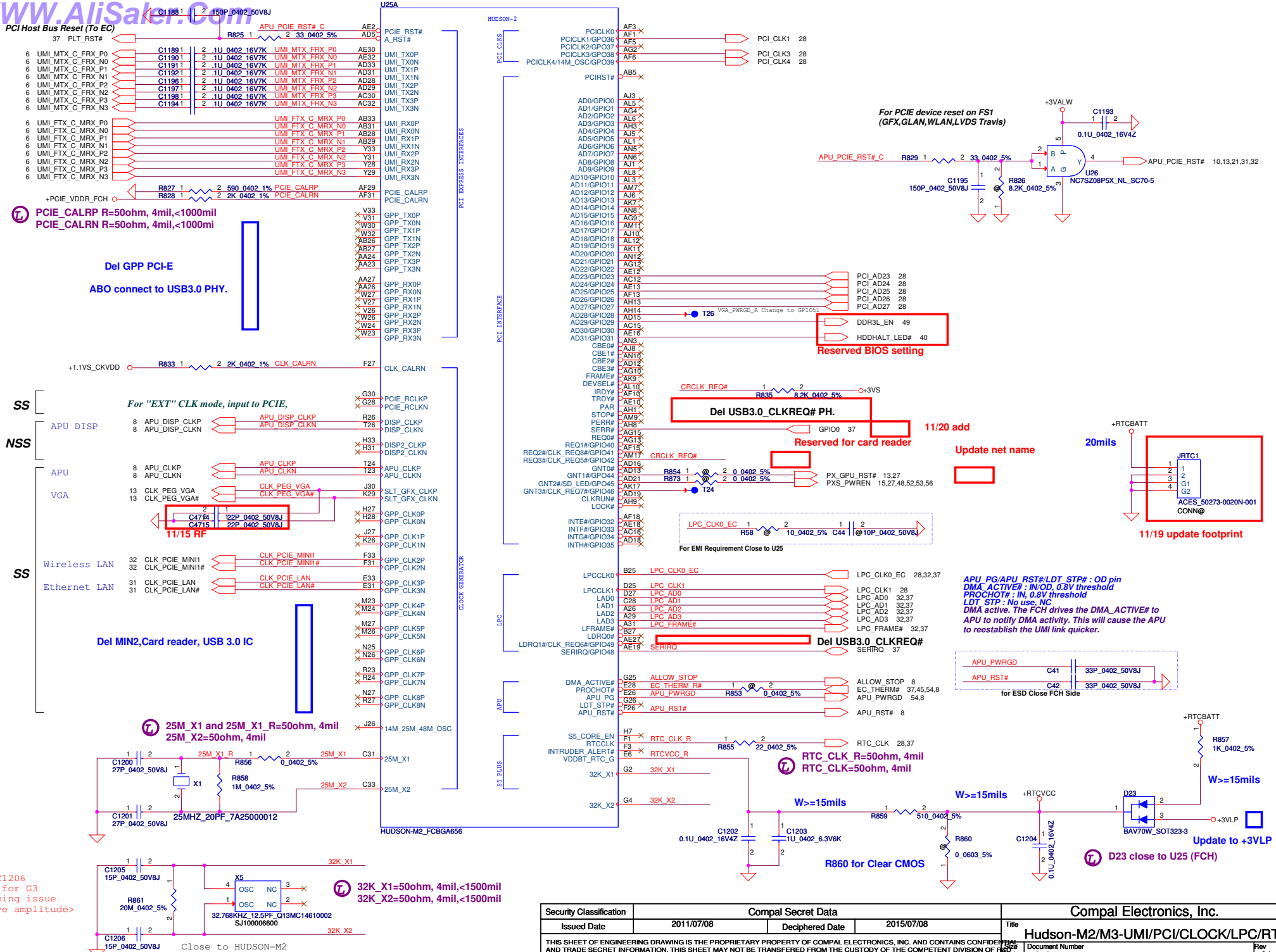


From APU

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				Date:	Monday, November 28, 2011
				Sheet	23 of 56
				Rev	0.1
				QCL51 LA-8712P	

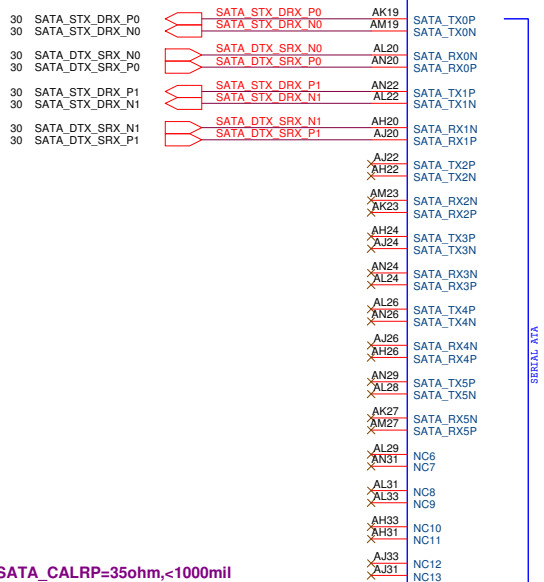


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Issued Date	2011/07/08	Deciphered Date	2015/07/08	Title	CRT Connector
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				Date:	Monday, November 28, 2011
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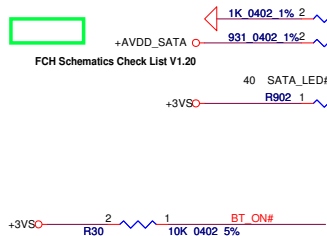


HDD1

ODD

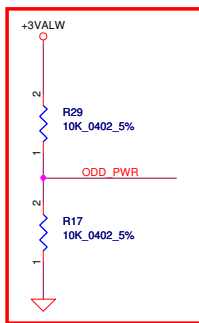


FCH Schematics Check List V1.20



Del\_WL\_Off#\_2

11/16 Follow Q5WV8  
 Del\_W\_DISABLE#\_2



11/15 AMD check list for reserved.

HUDSON-2

SERIAL ATA

HW MONITOR

HUDSON-M2\_FCBGA656



Check CS# R10 1k or 10k and pop/nopop  
 SCL v1.20: If an SPI ROM is shared between  
 the FCH and the Embedded Controller  
 a 10-K pull-up resistor to +3.3V\_S5 is installed.

GBE\_COL / GBE\_CRS / GBE\_MDIO  
 GBE\_RXERR / Left unconnected.  
 FCH SCL V1.20 19-35

**FCH\_SPI\_MISO** V6  
**FCH\_SPI\_MOSI** V5  
**FCH\_SPI\_CLK#** R35 1 2 0 0402 5%  
**FCH\_SPI\_CS#** V3  
**FCH\_SPI\_WP#** V1

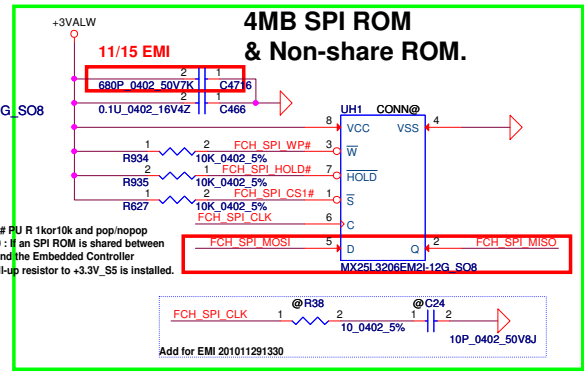
**FCH\_CRT\_R** L30  
**FCH\_CRT\_G** L32  
**FCH\_CRT\_B** M29  
**FCH\_CRT\_HSYNC** M28  
**FCH\_CRT\_VSYNC** N30  
**FCH\_CRT\_DDC\_SDA** M33  
**FCH\_CRT\_DDC\_SCL** N32  
**FCH\_CRT\_HPDP** C29

**ML\_VGA\_AUXP\_C** V28  
**ML\_VGA\_AUXN\_C** V29  
**AUXCAL** U28  
**ML\_VGA\_TXP0** T31  
**ML\_VGA\_TXN0** T33  
**ML\_VGA\_TXP1** T29  
**ML\_VGA\_TXN1** T28  
**ML\_VGA\_TXP2** R32  
**ML\_VGA\_TXN2** R30  
**ML\_VGA\_TXP3** P29  
**ML\_VGA\_TXN3** P28

**FCH\_CRT\_HPDP** C29  
**FCH\_CRT\_HPDP** 10 10K\_0402\_5%  
**FCH\_VDDAN\_33\_DAC\_R** R904

**NC1** AG16  
**NC2** AH10  
**NC3** A28  
**NC4** G27  
**NC5** L4

4MB SPI ROM  
 & Non-share ROM.



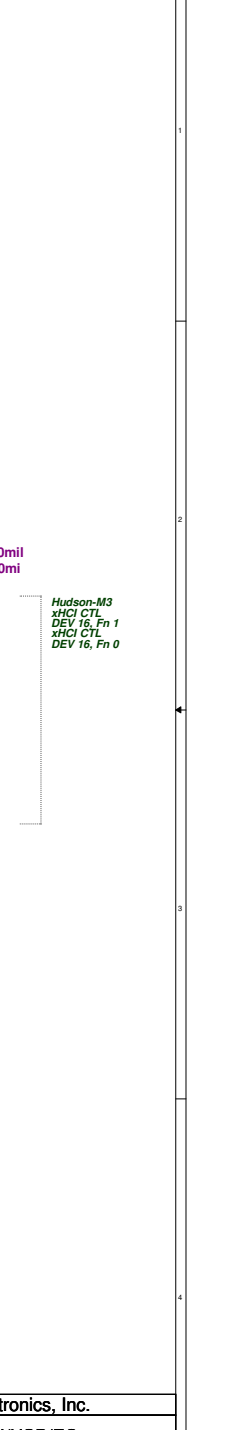
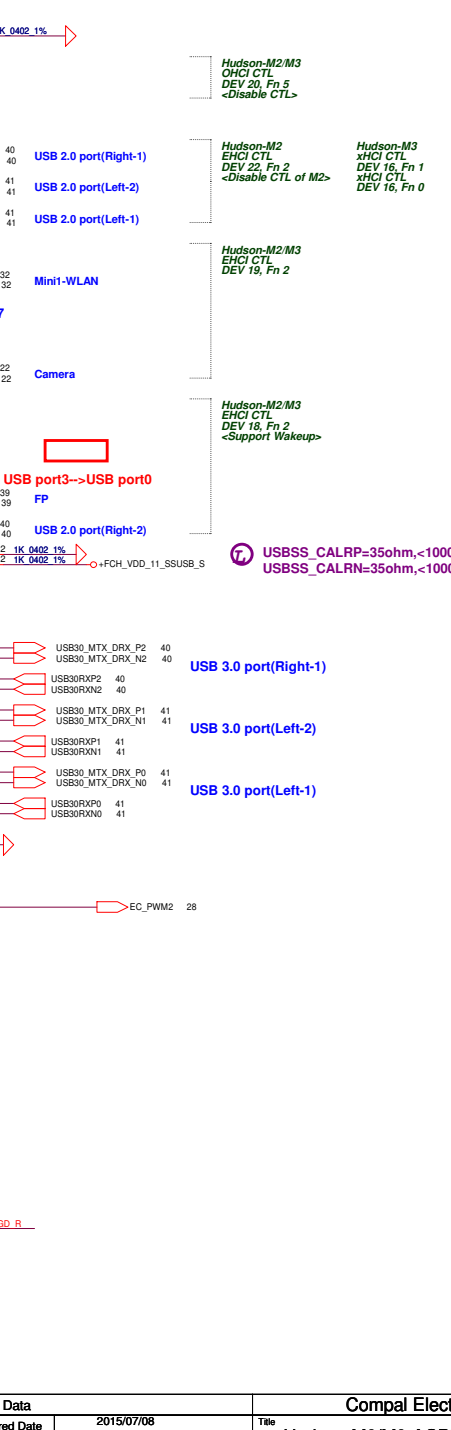
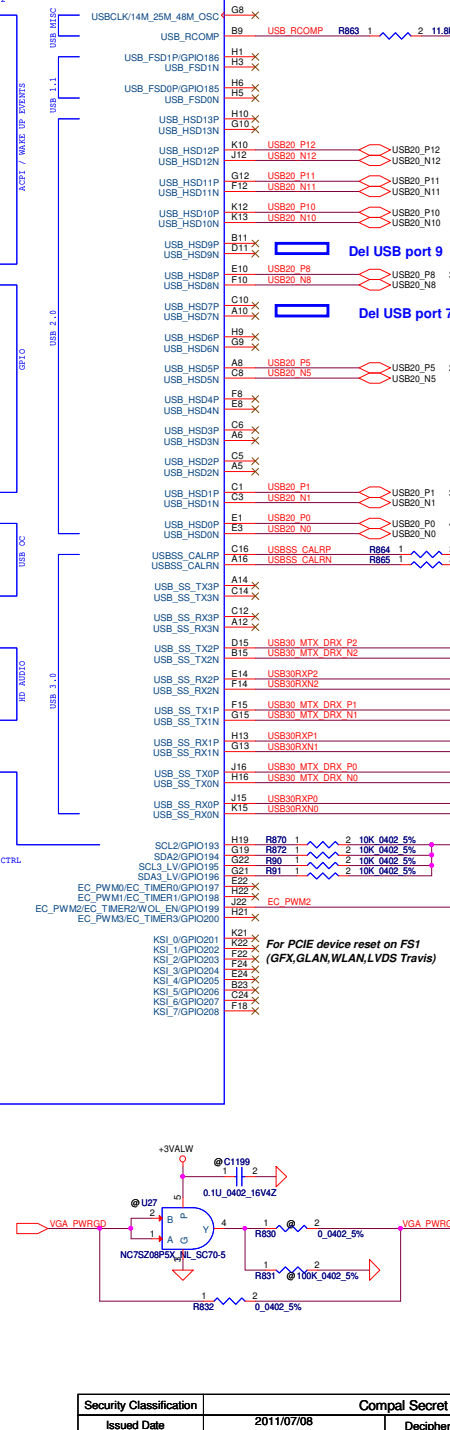
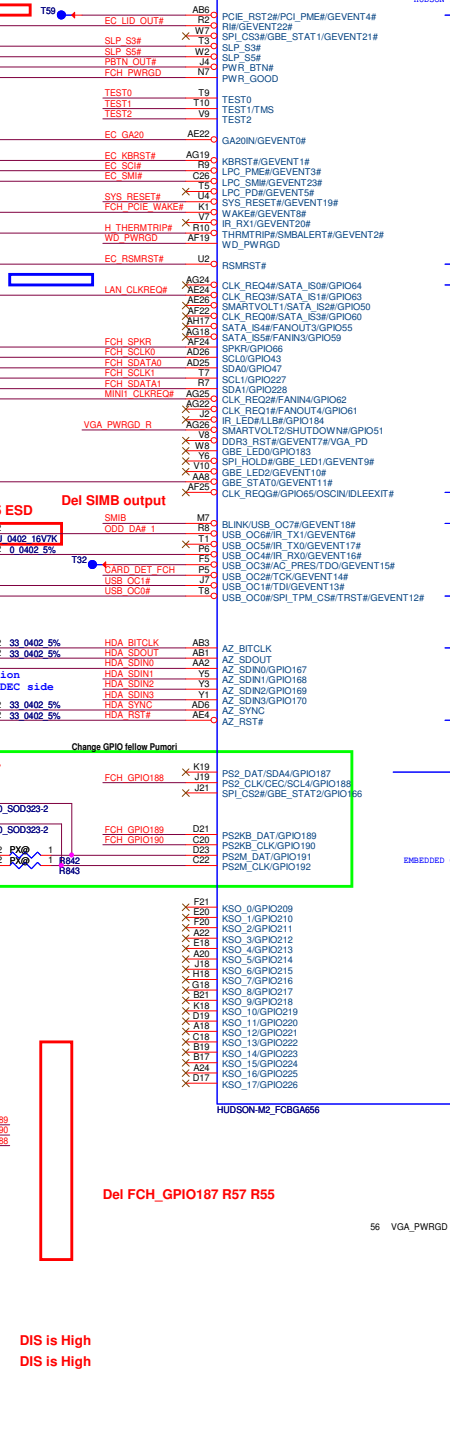
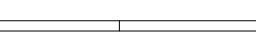
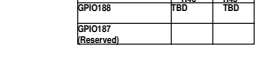
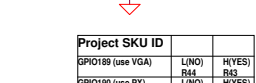
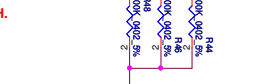
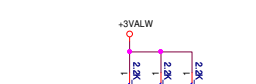
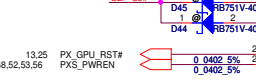
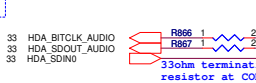
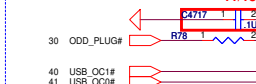
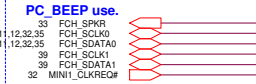
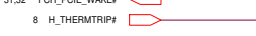
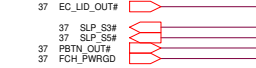
**GBE\_PHY\_INTR**  
 Pulled up to +3.3V\_S5 with a 10-K 5% resistor.  
 FCH SCL v1.20 #19-85  
**GBE\_PHY\_INTR** 1 10K\_0402\_5%  
 Removed RGMII/MII support and updated termination  
 requirements for GBE\_COL, GBE\_CRS, GBE\_RXERR  
 and GBE\_MDIO when RGMII/MII interface is not used.  
 FCH DGv1.20 / SCL v1.20

**AUXCAL <1000mil**

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Hudson-M2/M3-SATA/GBE/HWM				Monday, November 28, 2011
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FCH\_PCIE\_RST# IS FOR PCIE DEVICES ON Hudson-M2/M3

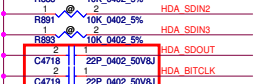
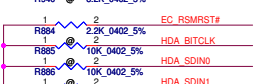
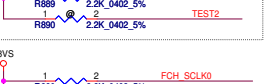
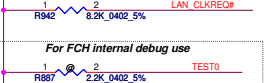
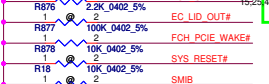
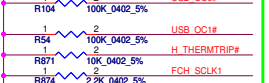
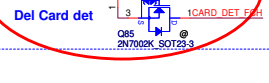
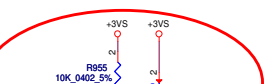
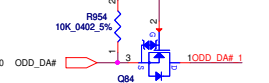
Del FCH\_PCIE\_RST#



ThermTRIP:  
Need level shift from +3VALW to +1.5V  
Note: Ensure FCH internal pull-up resistor to +3.3V S5 is disabled to prevent leakage when APU is powered down.

SM bus 0-->S5 PWR domain  
SM bus 1-->S5 PWR domain

FCH\_GEVENT (S5 domain)  
with isolation circuit to avoid leakage



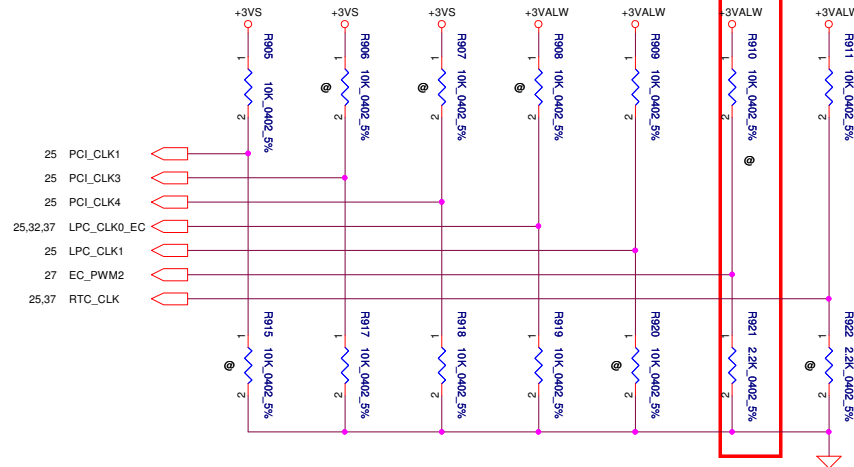
Project SKU ID		
GPI0189 (use VGA)	LW0	HYES
GPI0190 (use PX)	LW0	HYES
GPI0188	R4	R4
GPI0187 (Reserved)	R4	R4

DIS is High  
DIS is High

Change to SPI

## STRAP PINS

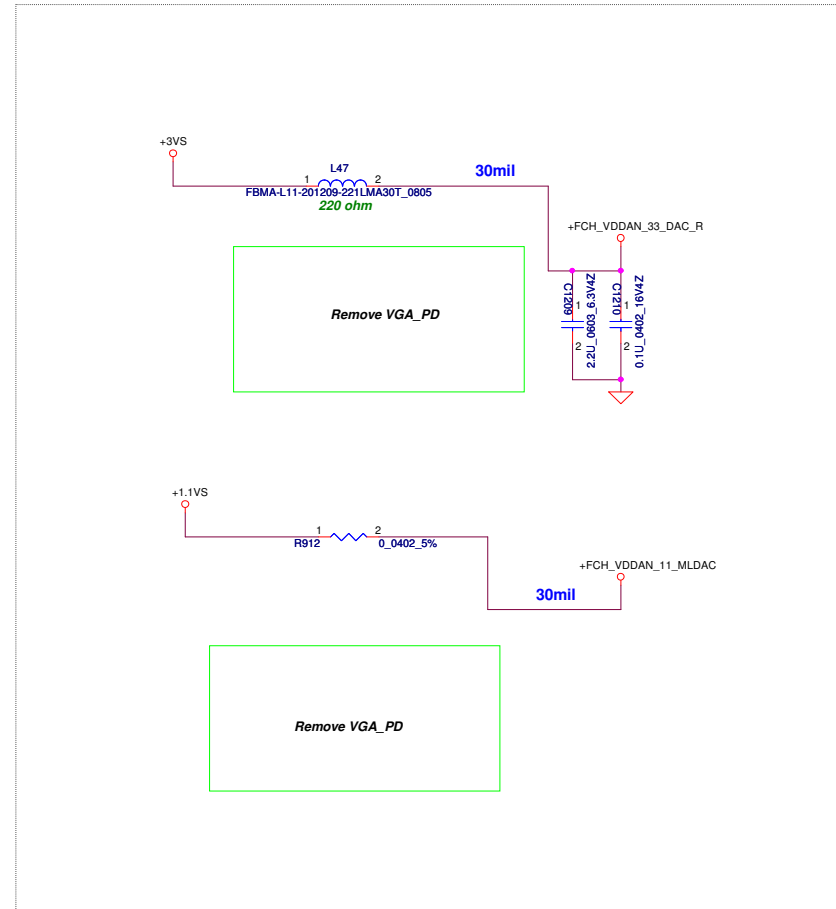
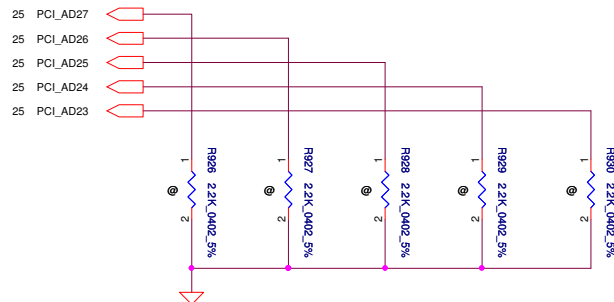
	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM DEFAULT	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM	S5 PLUS MODE ENABLED



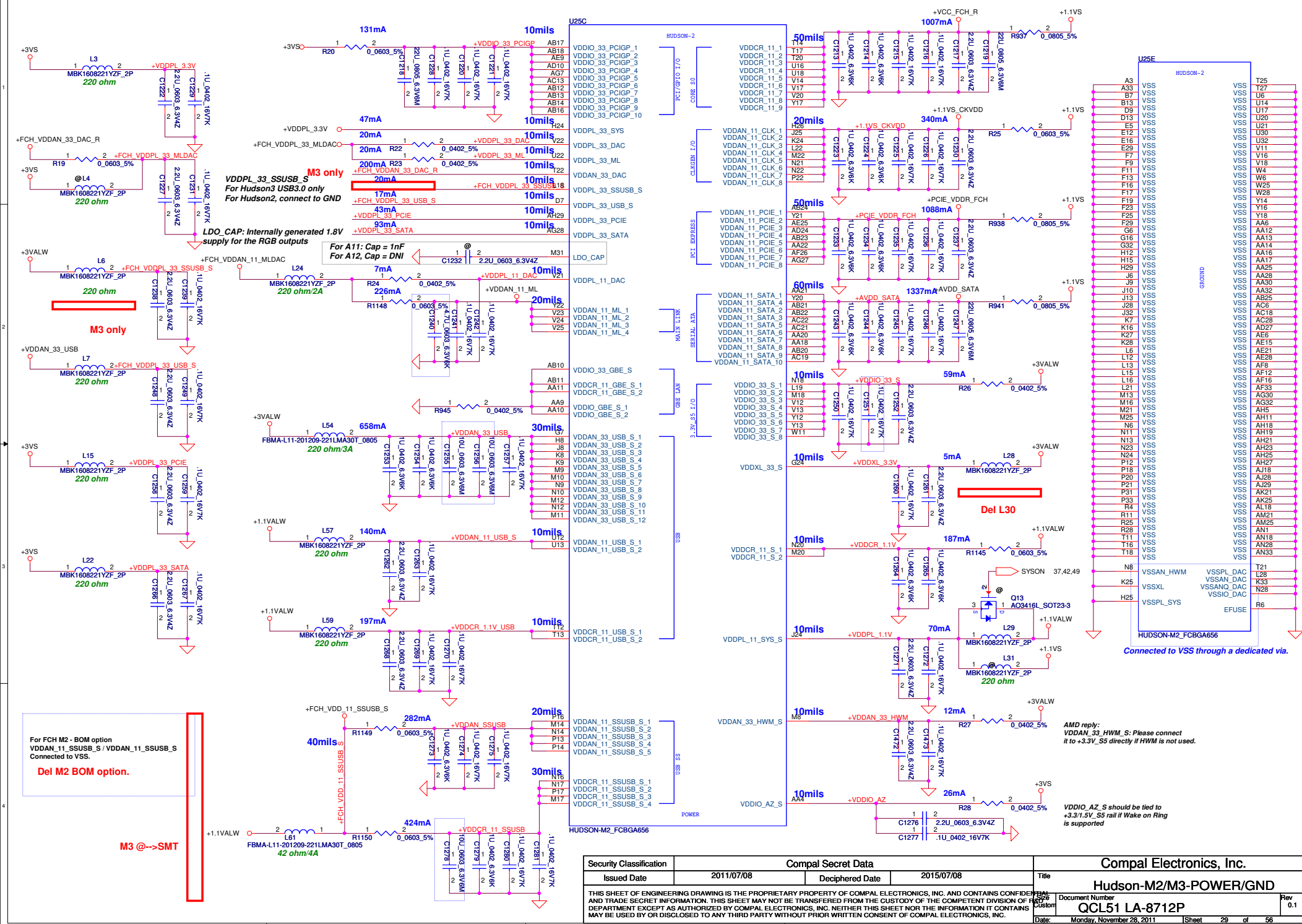
## DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI\_AD[27:23]

	PCI_AD27	PCI_AD25	PCI_AD24	PCI_AD23
No external R	USE PCI PLL DEFAULT	Normal REFCLK termination DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	Inverted REFCLK termination	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



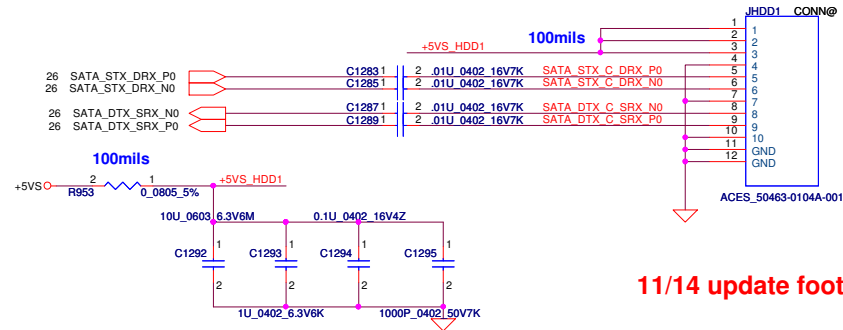




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				Part Number Document Number Revision	QCL51 LA-8712P Date: Monday, November 28, 2011 Sheet 29 of 56

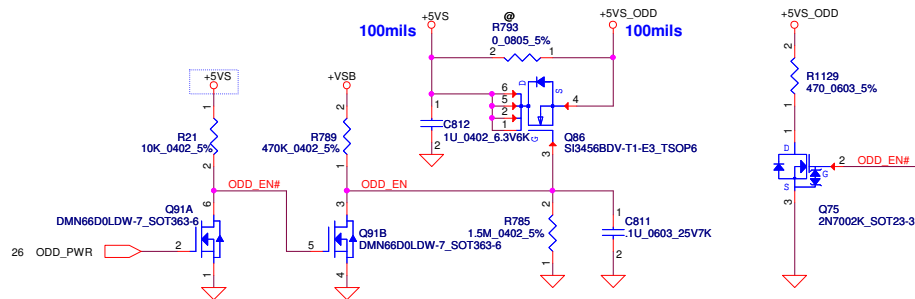


# SATA HDD1 Conn.



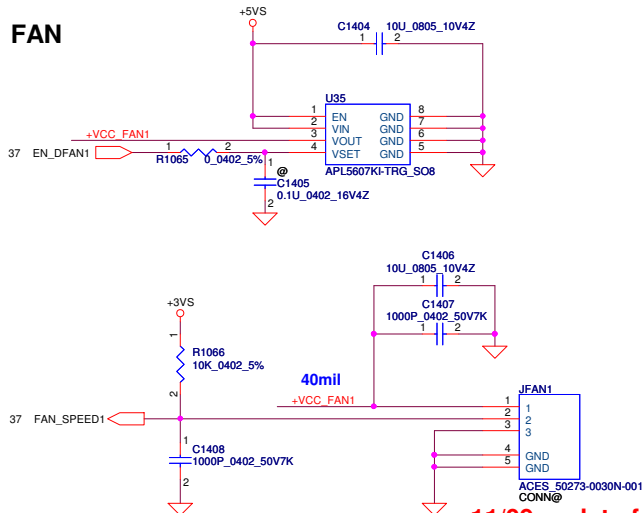
11/14 update footprint

## ODD conn



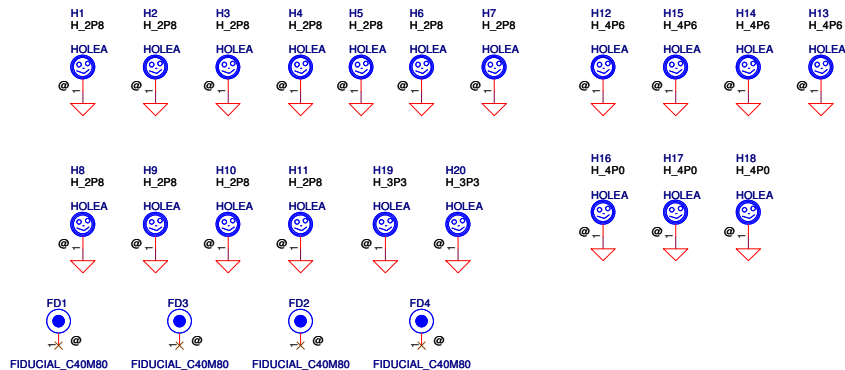
11/05 update footprint

## FAN



11/09 update footprint to VT.

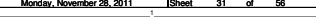
## Screw Hole



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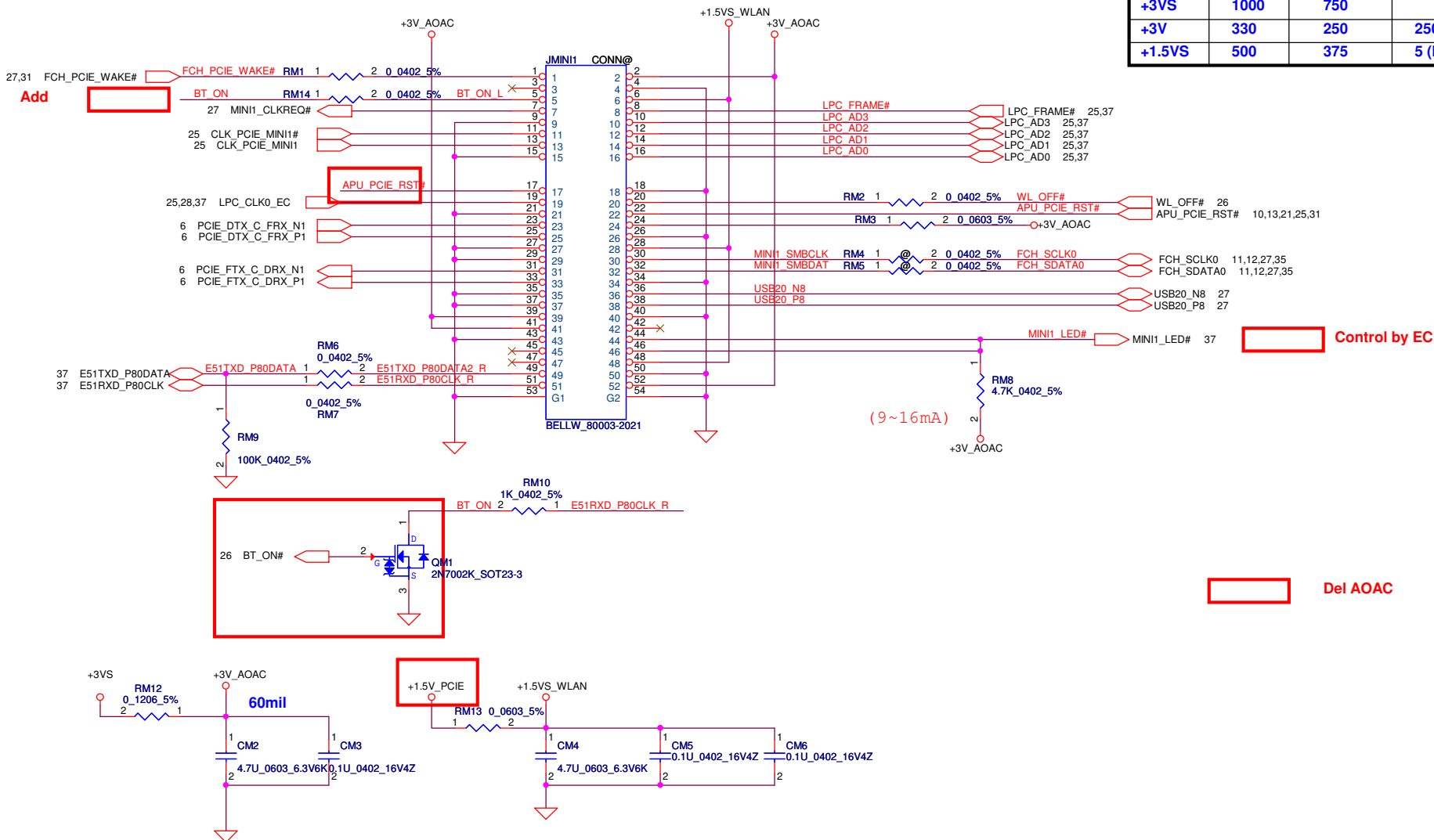


### Modify by Project



## WLAN

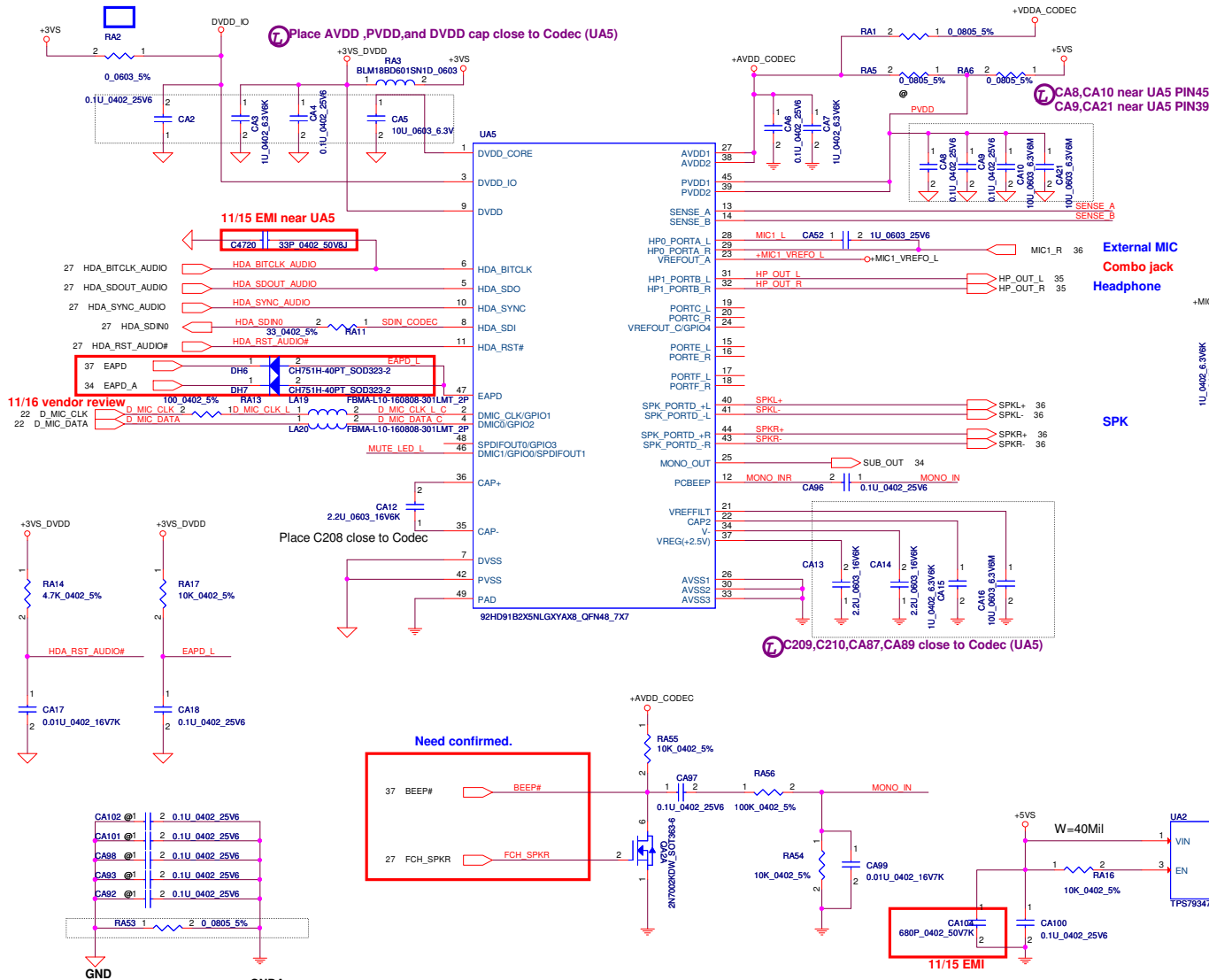
Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)



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				B	QCL51 LA-8712P	0.1
				Date:	Monday, November 28, 2011	Sheet 32 of 56

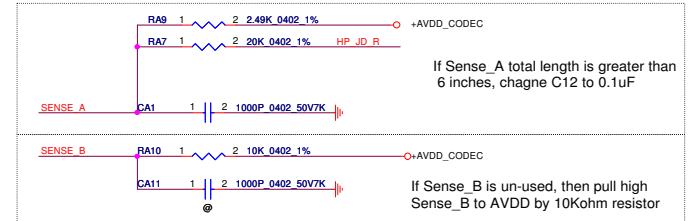
RA2 0805-->0603

Place AVDD, PVDD, and DVDD cap close to Codec (UA5)

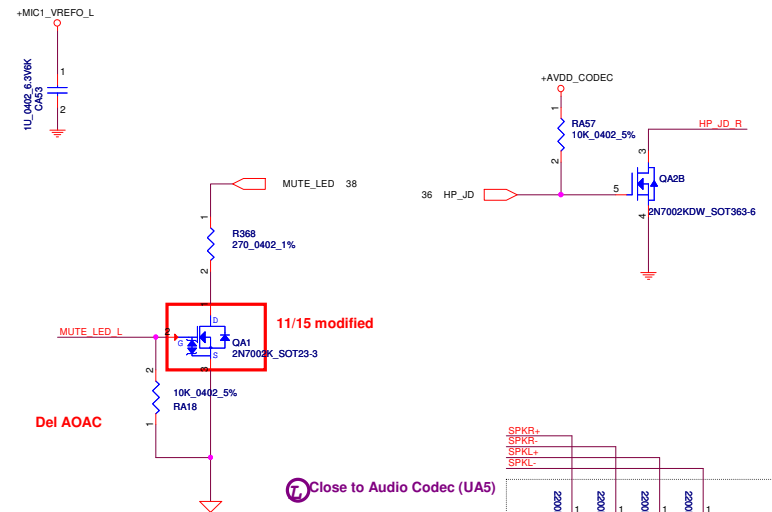


Notes:  
Keep PVDD supply and speaker traces routed on the DGND plane.  
Keep away from AGND and other analog signals

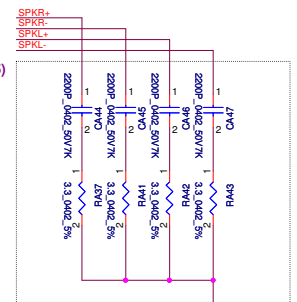
PLACE CLOSE TO UA5 PIN 13



PLACE CLOSE TO UA5 PIN 14



Close to Audio Codec (UA5)

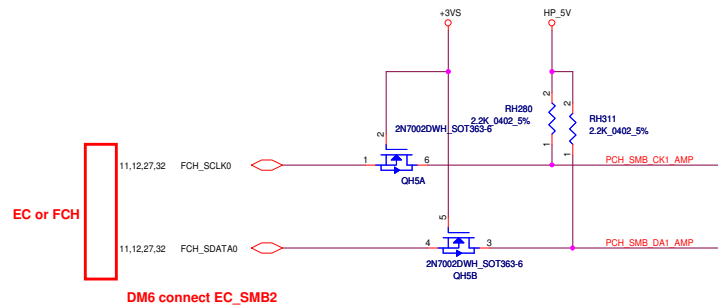
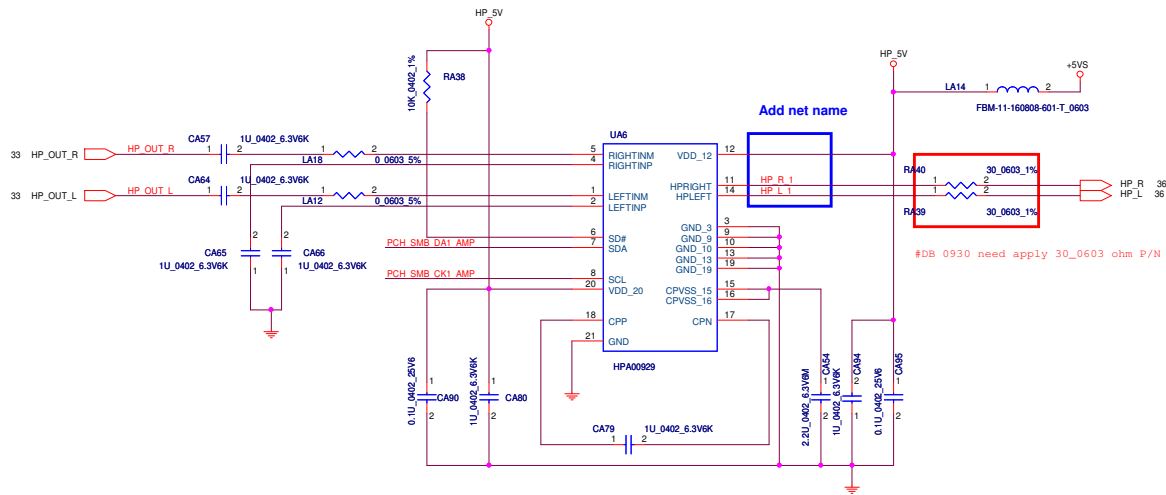


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				Custom	LA-8551P
				Date	Monday, November 28, 2011
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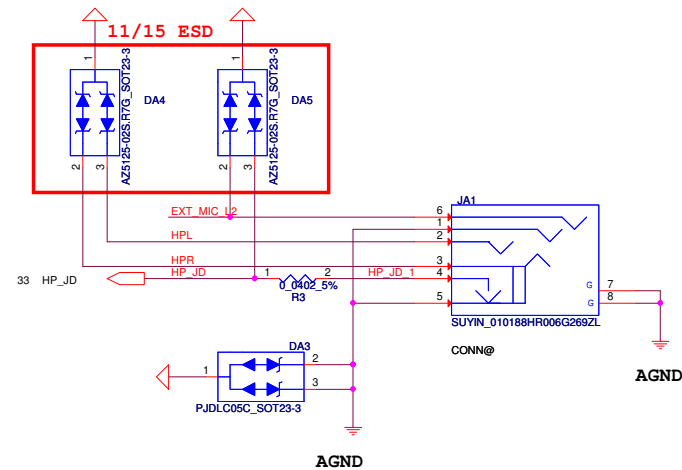
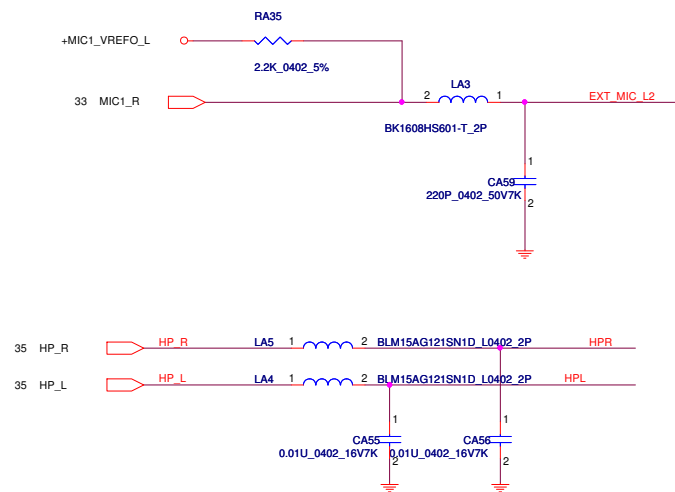
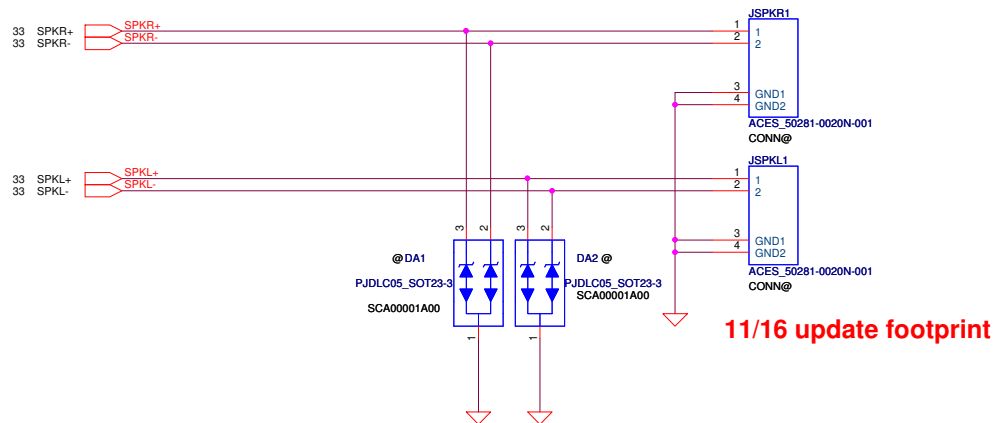


1

# Headphone amplifier

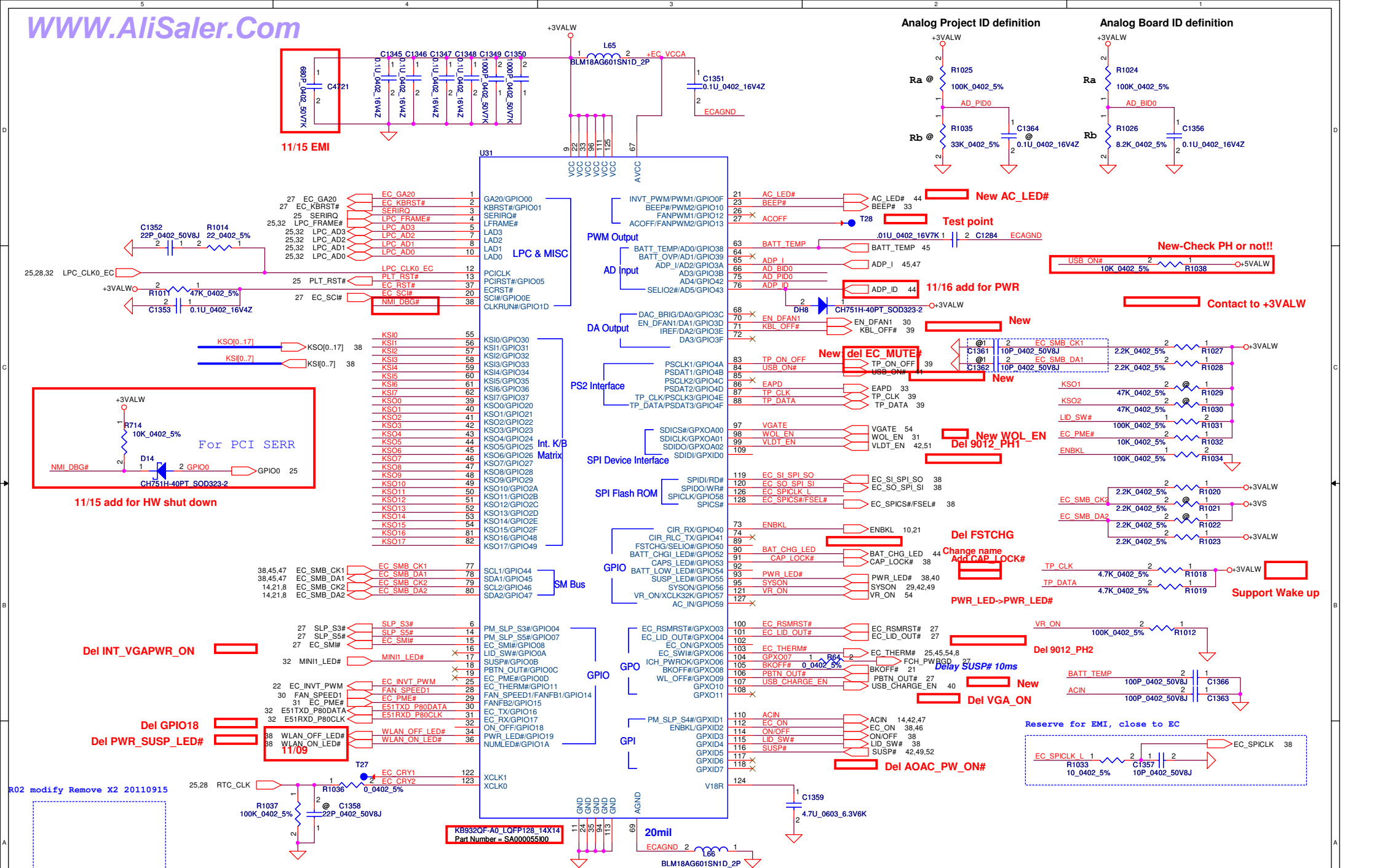


SPK conn



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Issued Date				2009/04/07				Deciphered Date			
2012/10/21				Title				Audio SPK Conn/Jack/MIC			
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QCL51 LA-8712P				Date				Monday, November 28, 2011			
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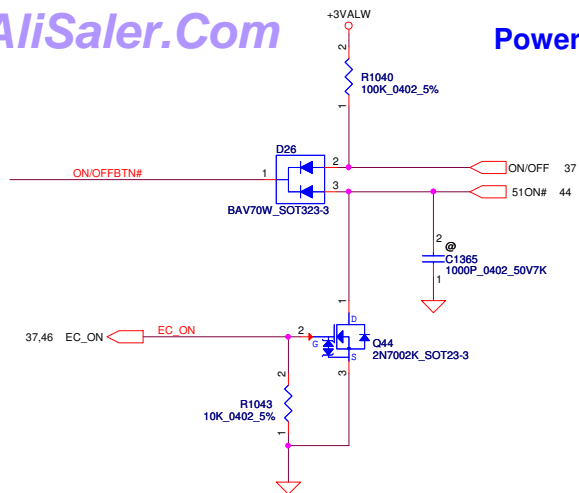




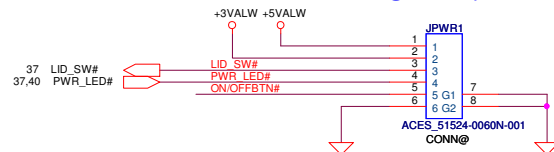
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Issued Date	2011/07/08	Deciphered Date	2015/07/08	Title	
				EC ENE KB930/9012	
				Size	Document Number
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## Power Button

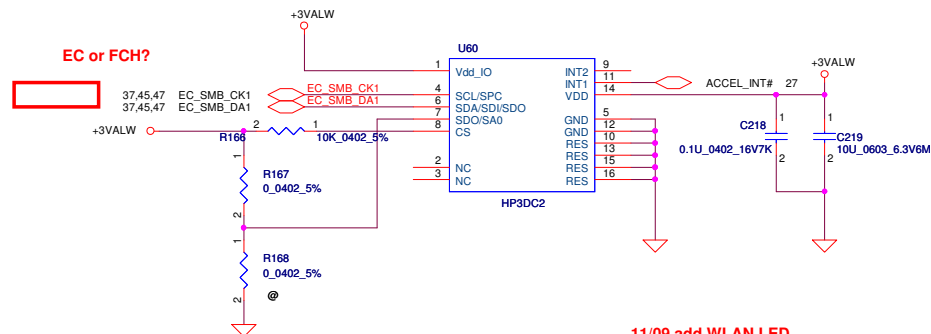


## POWER/B

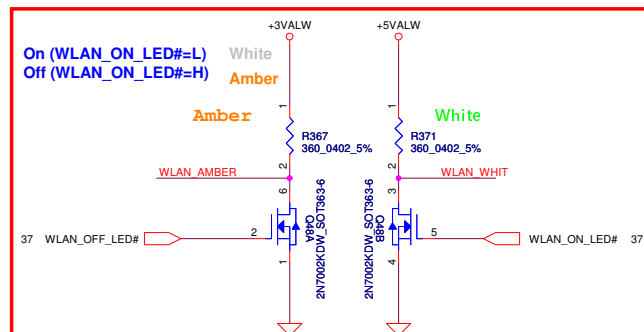


11/05 update footprint

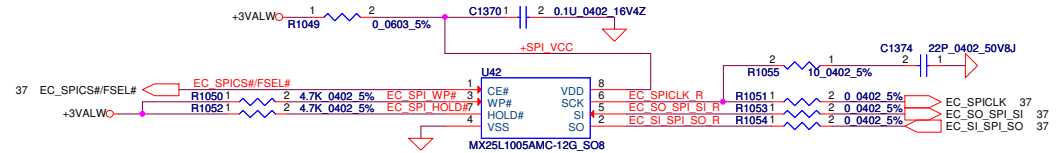
## ACCELEROMETER



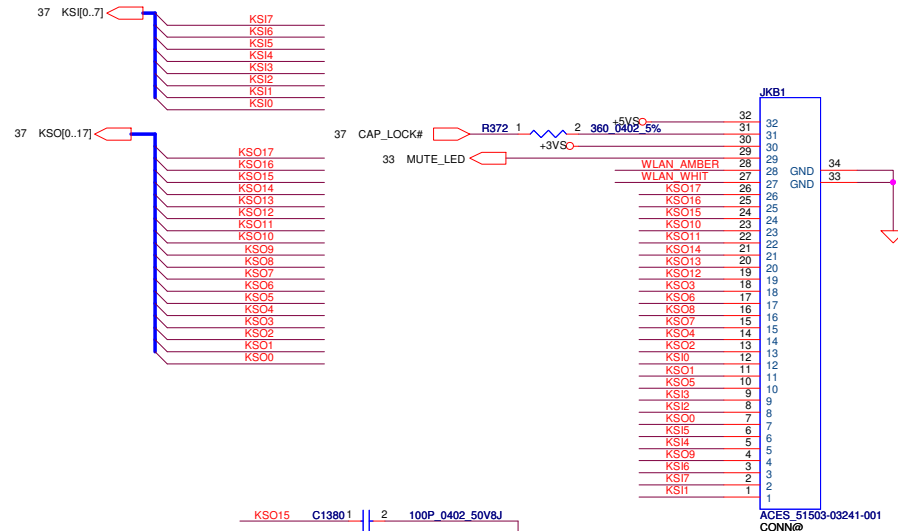
11/09 add WLAN LED



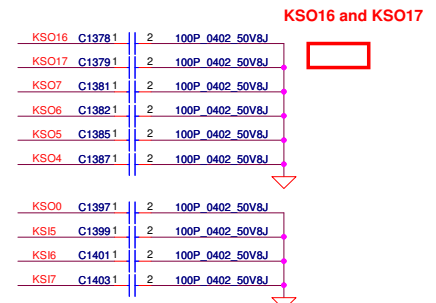
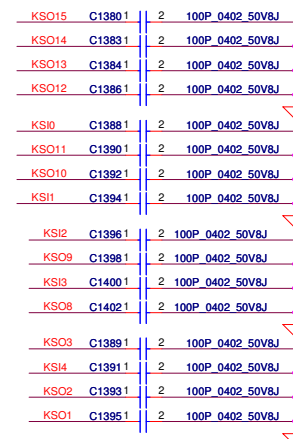
## EC BIOS ROM



## KB conn

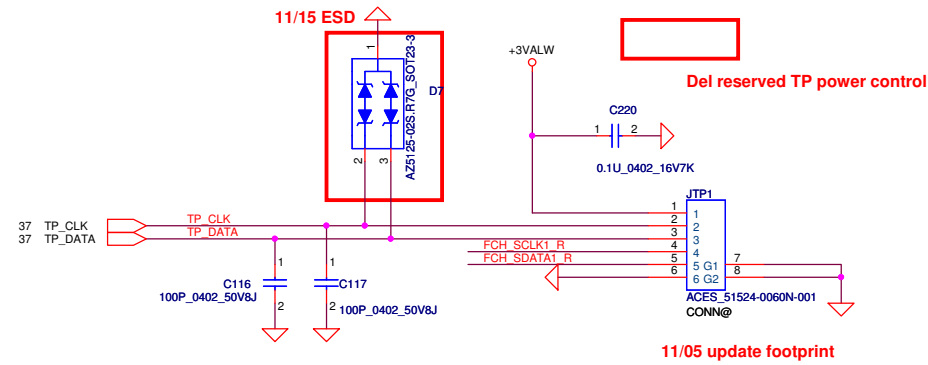


11/05 update footprint

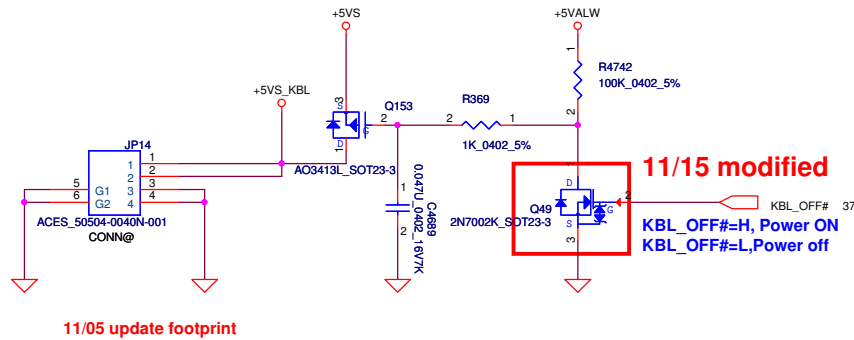


Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2011/07/08				Deciphered Date			
2015/07/08				2015/07/08				Title			
BIOS, I/O Port & K/B CONN/TP CONN/PBTN				Document Number				Rev			
QCL51 LA-8712P				0.1				Date			
Monday, November 28, 2011				Sheet				38 of 56			

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### Keyboard backlight Conn

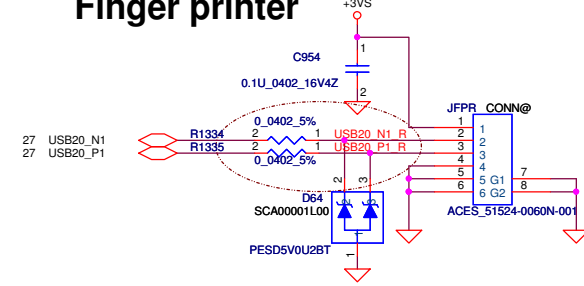


### AOAC power control

Del AOAC

### Finger printer

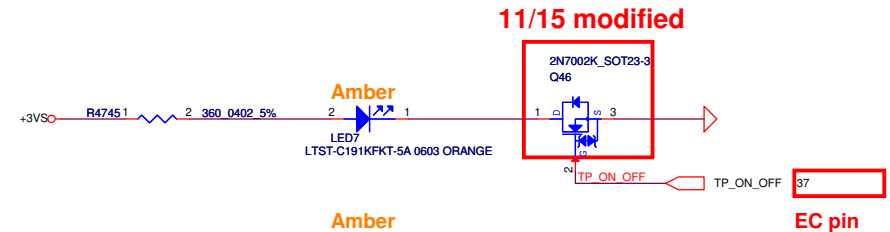
Will change to 8 pins



### WLAN ON/OFF LED

11/09 Change to KB connector

### T/P On/Off LED

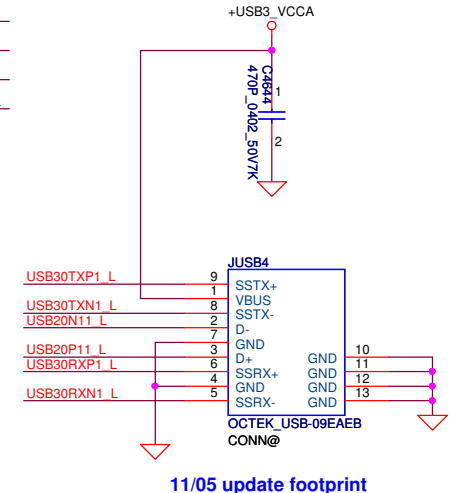
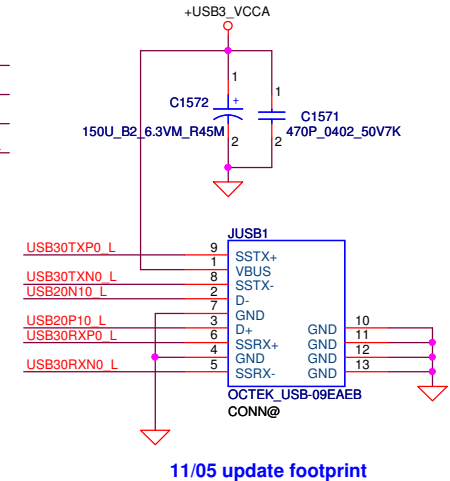
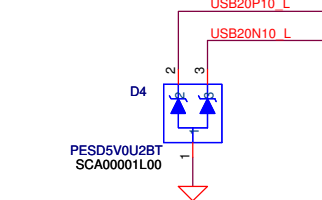
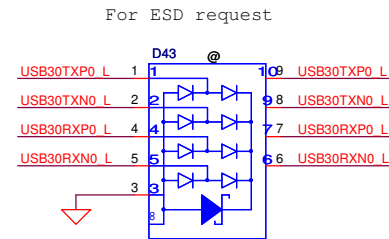
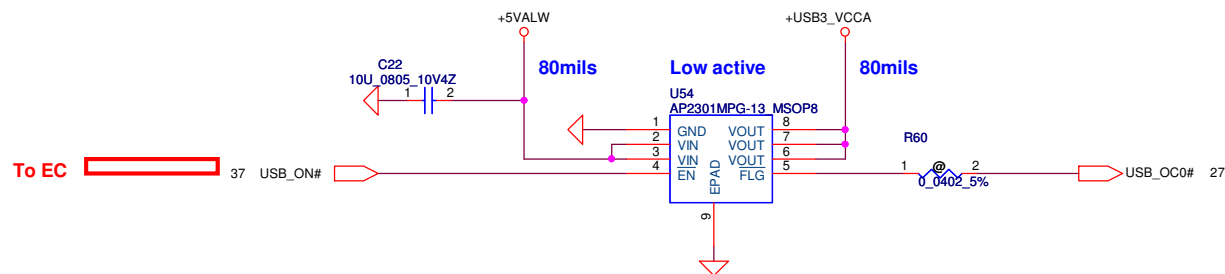
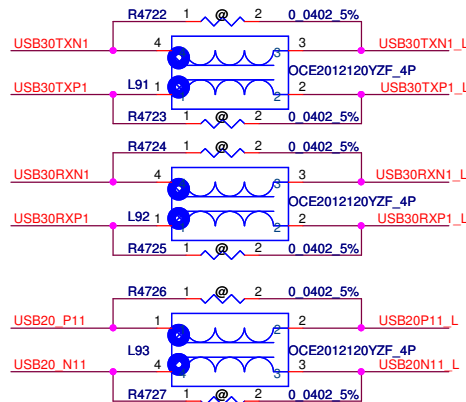
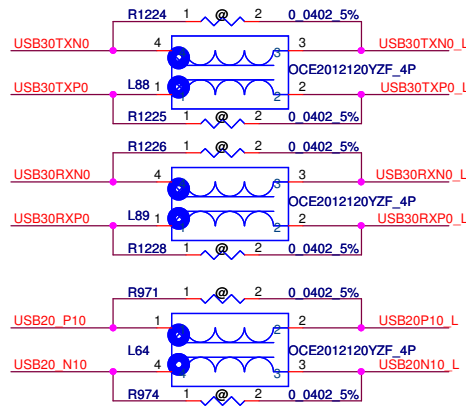
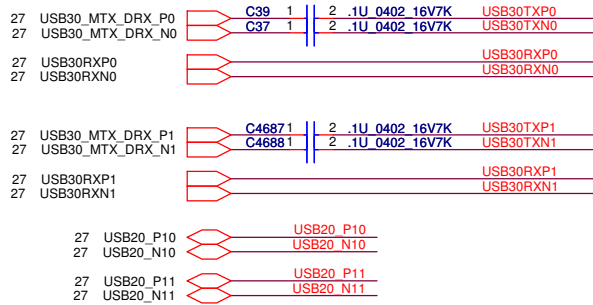


### Mute On/Off LED

11/09 Change to KB connector

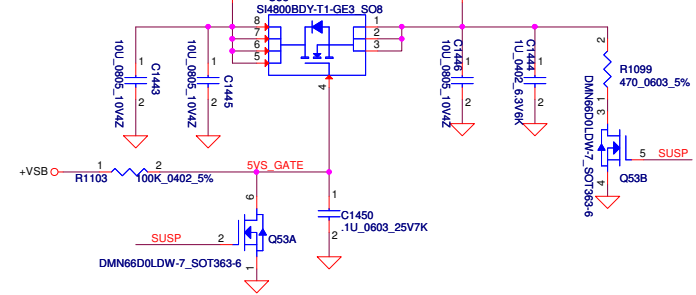
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Issued Date	2011/07/08	Deciphered Date	2015/07/08	Title	LAN Magnetic & RJ45
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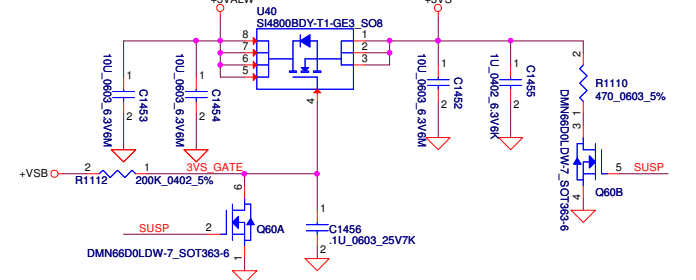


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				Date: Monday, November 28, 2011	Sheet 41 of 56

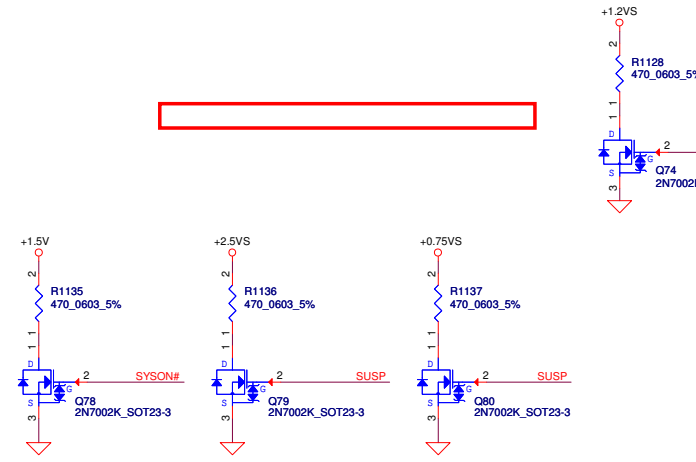
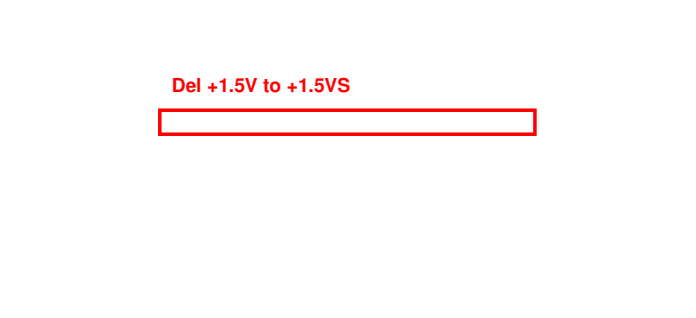
**+5VALW TO +5VS (5A)**



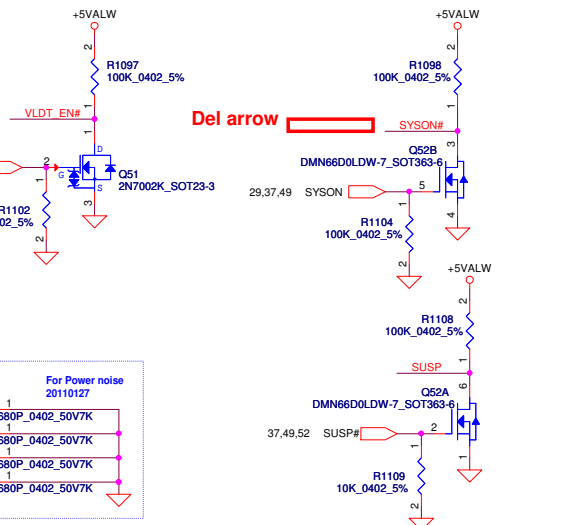
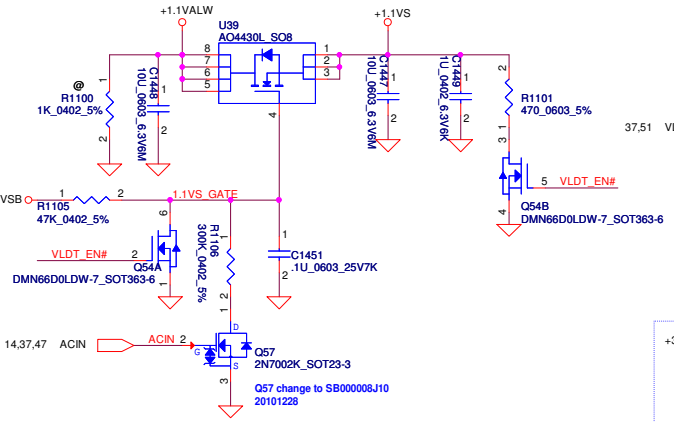
**+3VALW TO +3VS (3.3A)**



**+1.5V TO +1.5VS (1.5A)**



**+1.1VALW TO +1.1VS (1.1A)**



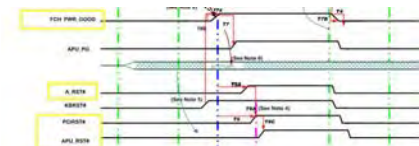
**VGA Power**

**+1.5V to +1.5VSG (1.5A)**

Del +1.5VSG and reserved on GPU

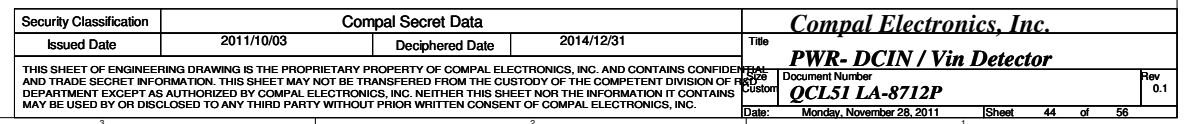
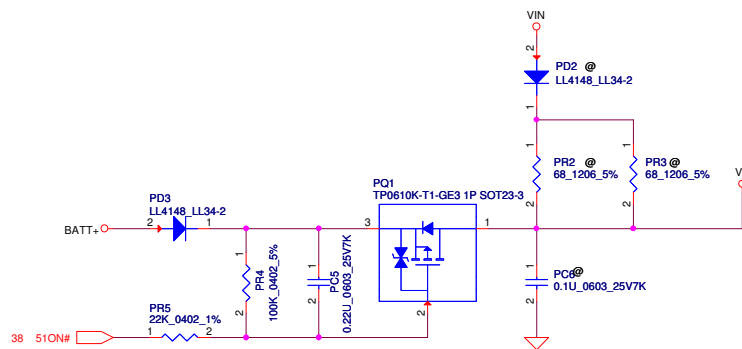
Del +3VSG and reserved on GPU

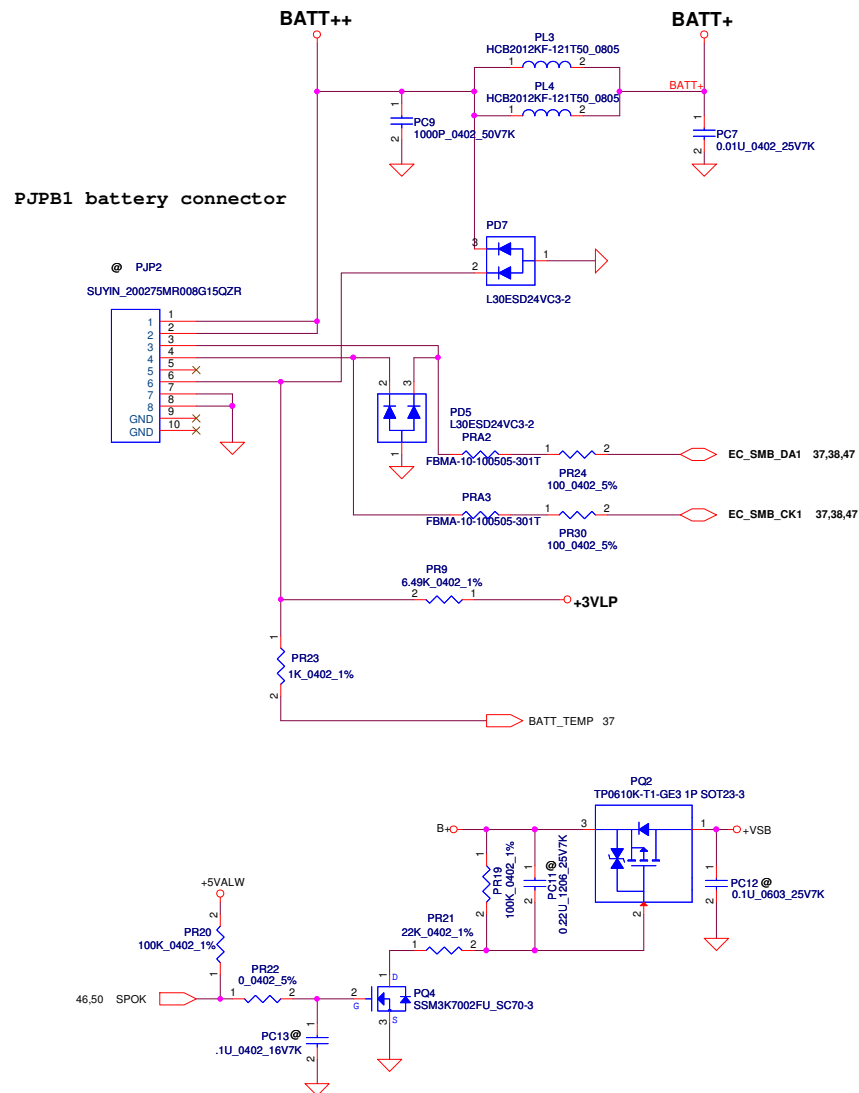
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Issued Date		2011/07/08		Deciphered Date		2015/07/08		Title			
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								Document Number		Rev	
								QCL51 LA-8712P		0.1	
								Date: Monday, November 28, 2011		Sheet 42 of 56	



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Issued Date 2011/07/08		Declassified Date 2015/07/08		Title DC Interface	
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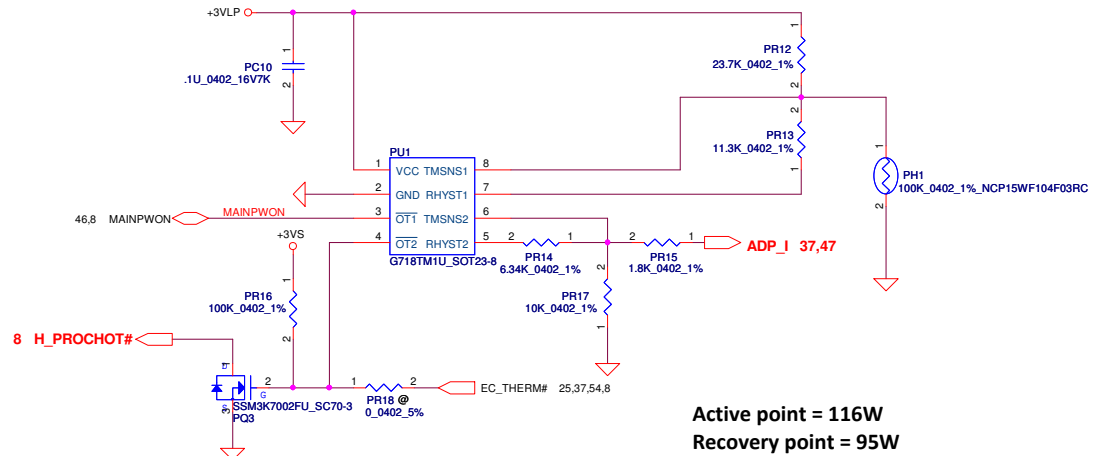




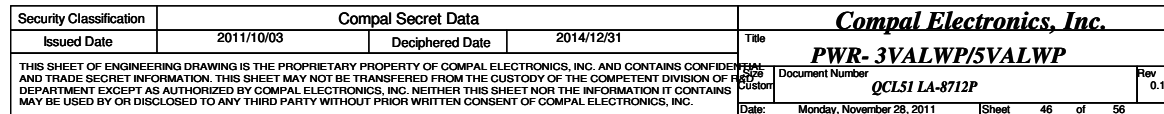
For KB930 --> Keep PU1 circuit  
(Vth = 0.825V)

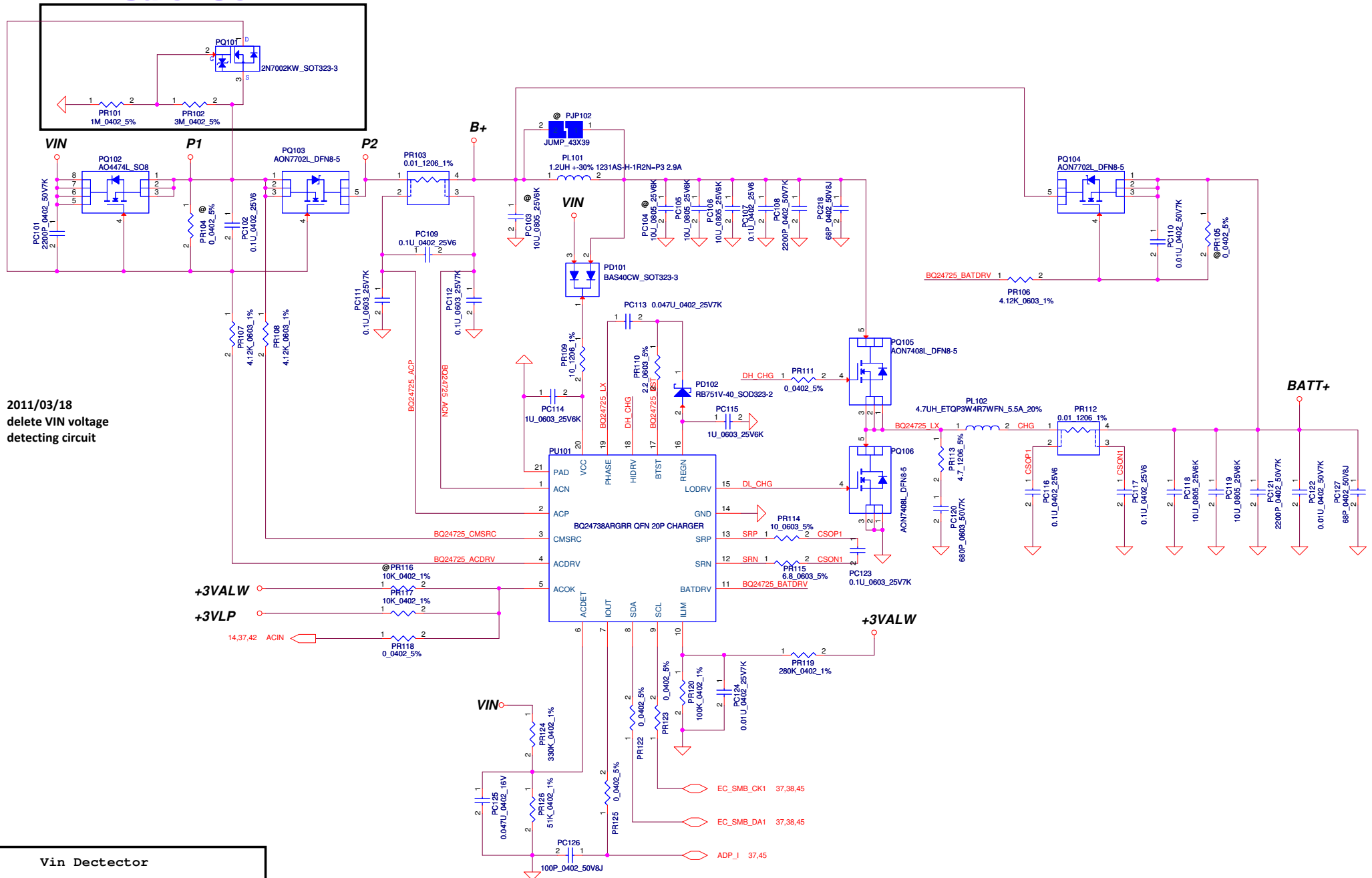
PH1 under CPU botten side :  
CPU thermal protection at 90 +-3 degree C  
Recovery at 56 +-3 degree C

Rset = 3 \* Rtmh  
Rhyst = (Rset \* Rtml) / (3 \* Rtml - Rset)  
Rtmh at 90C = 7.8K, Rtml at 56C = 26.1K  
Rset = 3 \* 7.8K = 23.4K ==> 23.7K  
Rhyst = (23.4K \* 26.1K) / (3 \* 26.1K - 23.4K) = 11.12K ==> 11.3K



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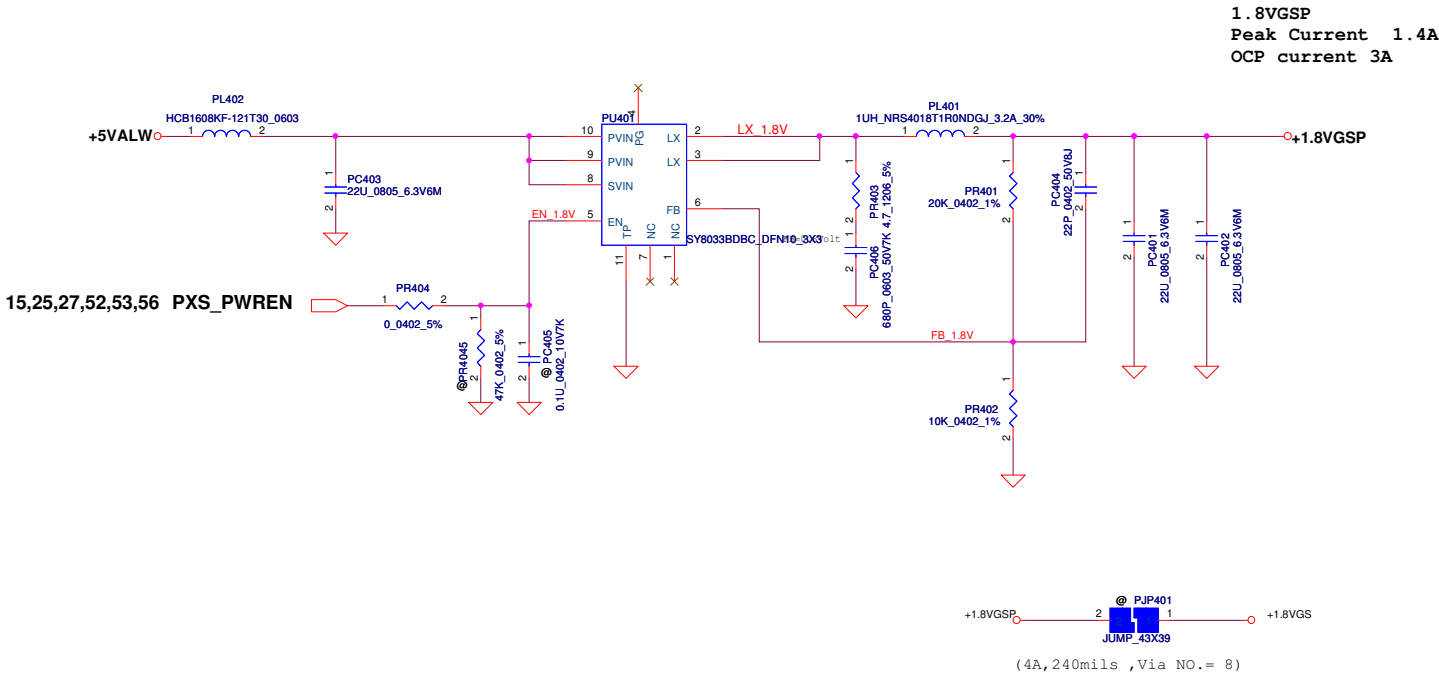
2011/03/18  
delete VIN voltage  
detecting circuit

#### Vin Detector

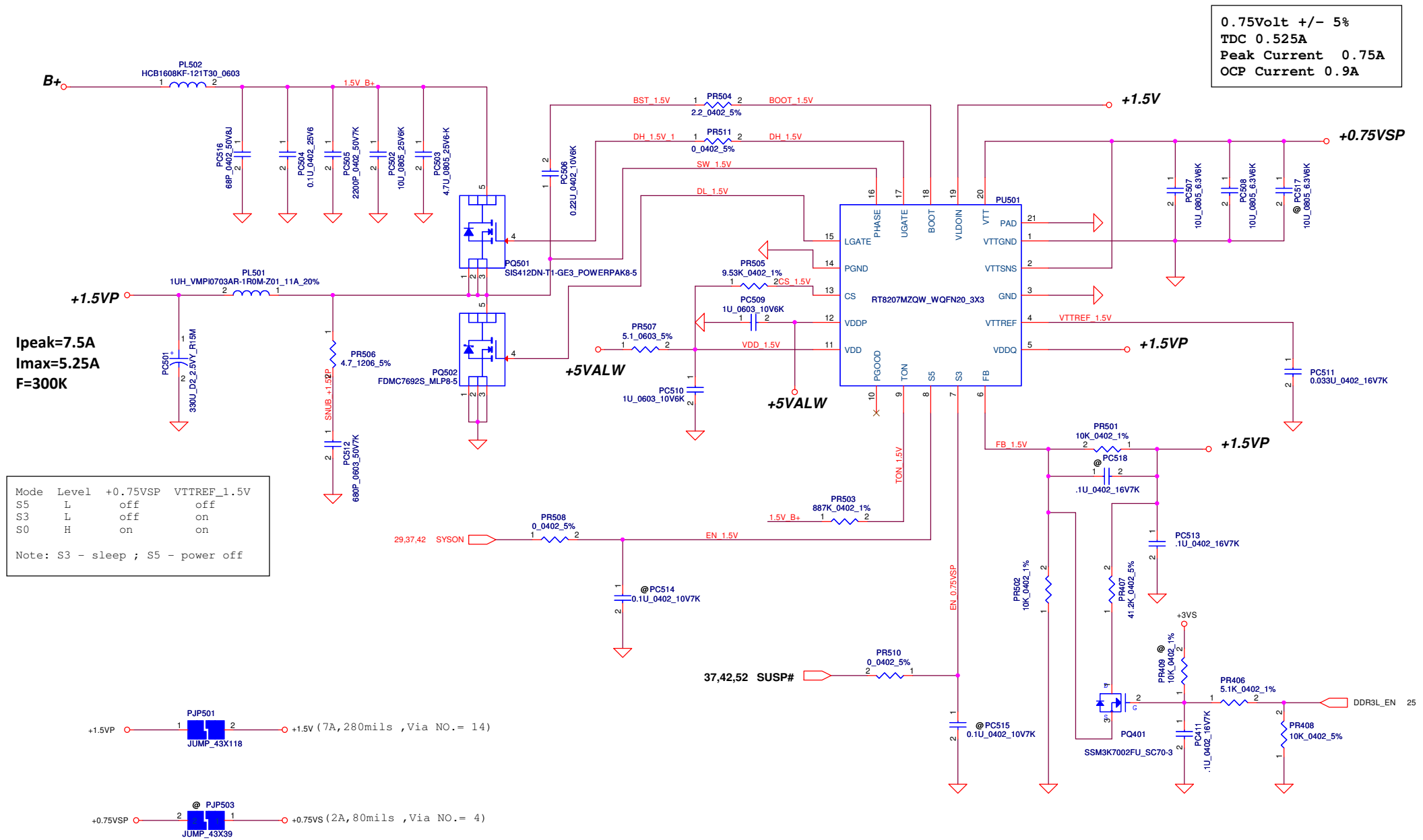
	Min.	Typ	Max.
H-->L		17.33V	
L-->H		16.98V	

ILIM and external DPM  
4.36A

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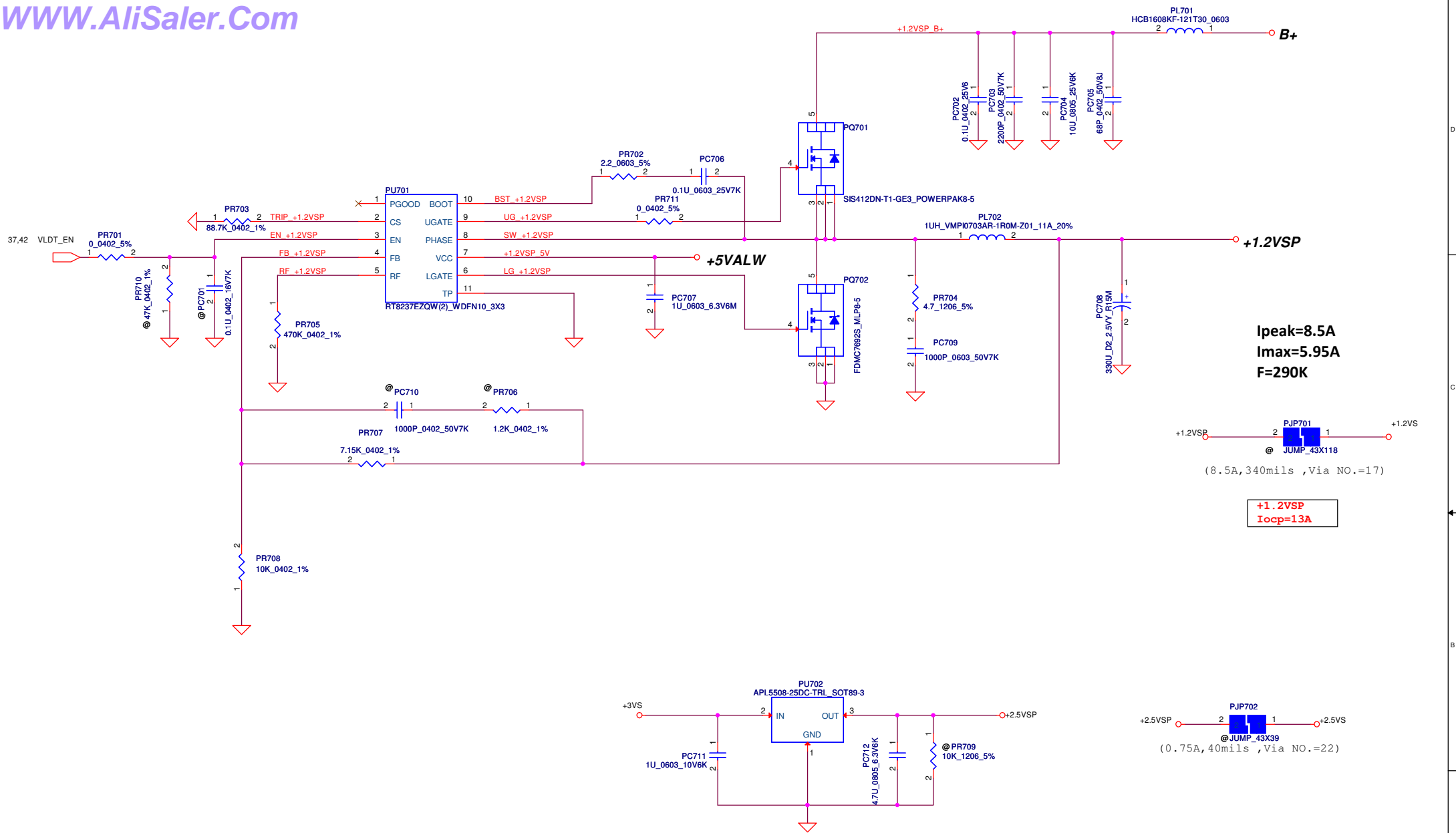
Security Classification		Compal Secret Data		Title	
Issued Date	2011/07/29	Deciphered Date		+1.8VP	
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Size	Document Number	Rev		0.1	
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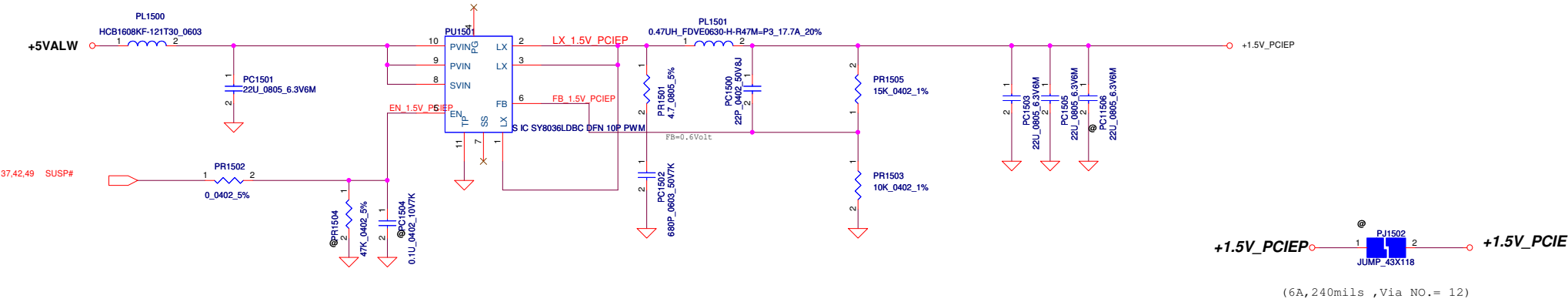




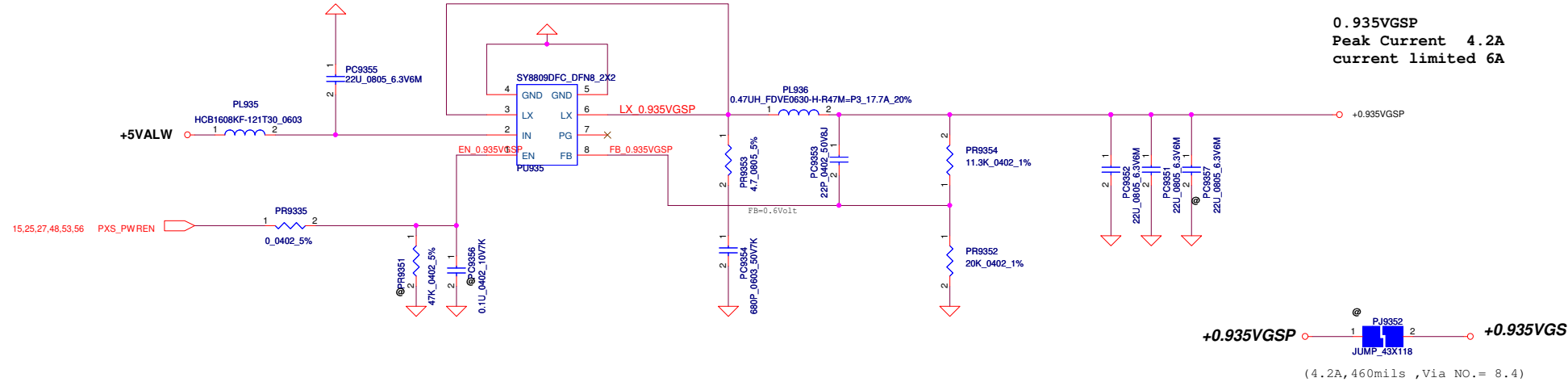


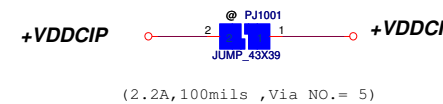
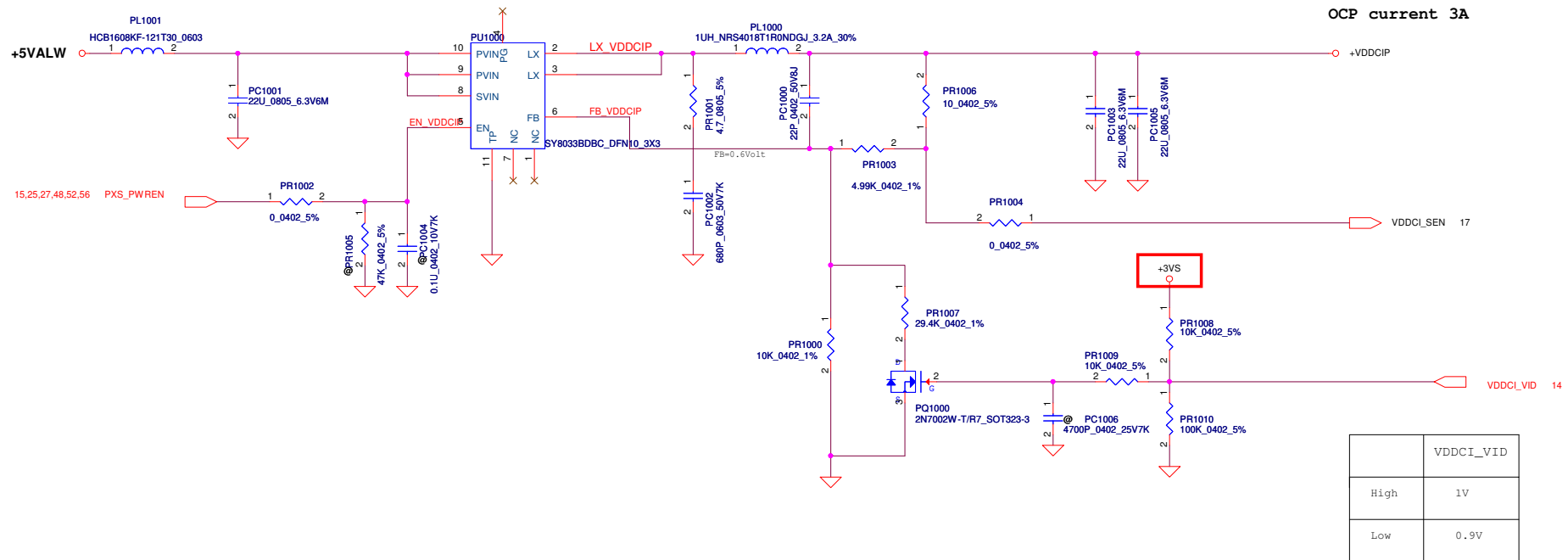
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1.5VPCIEP  
Peak Current 6A  
OCP current 6A

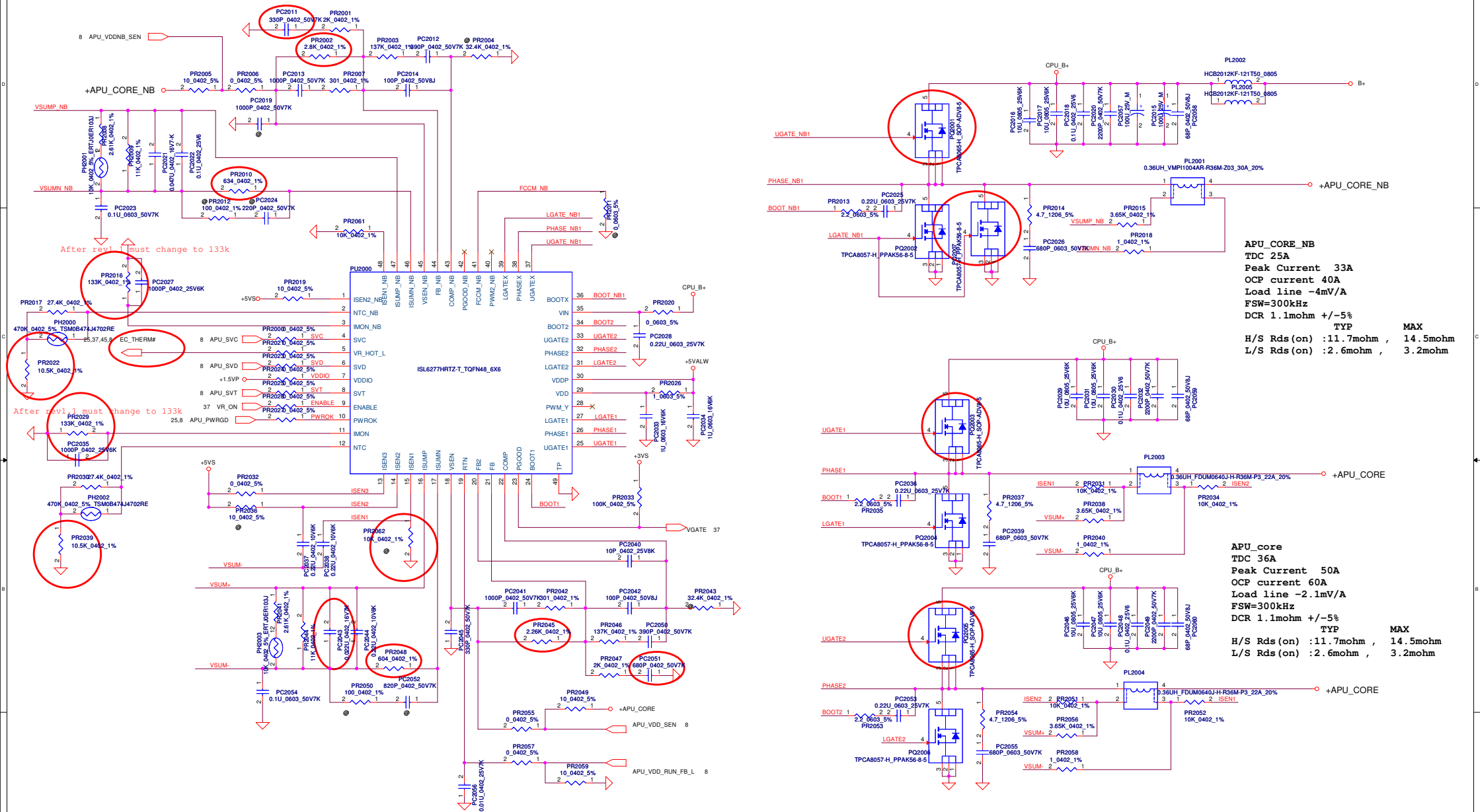


0.935VGSP  
Peak Current 4.2A  
current limited 6A





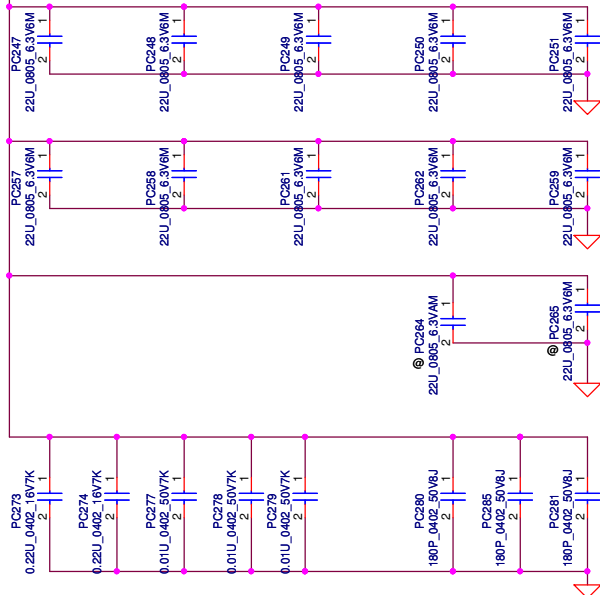
	VDDCI_VID
High	1V
Low	0.9V



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				Size Custom	Document Number
Date: Monday, November 28, 2011		Sheet 54 of 56			

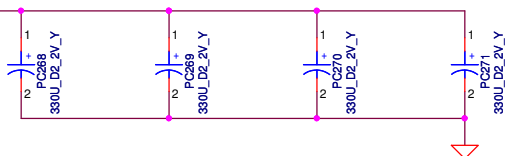
# +APU\_CORE

## +APU\_CORE



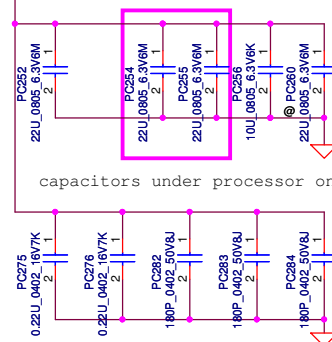
## +APU\_CORE

Local



# +APU\_CORE\_NB

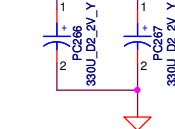
## +APU\_CORE\_NB



capacitors under processor on bottom side of board

## +APU\_CORE\_NB

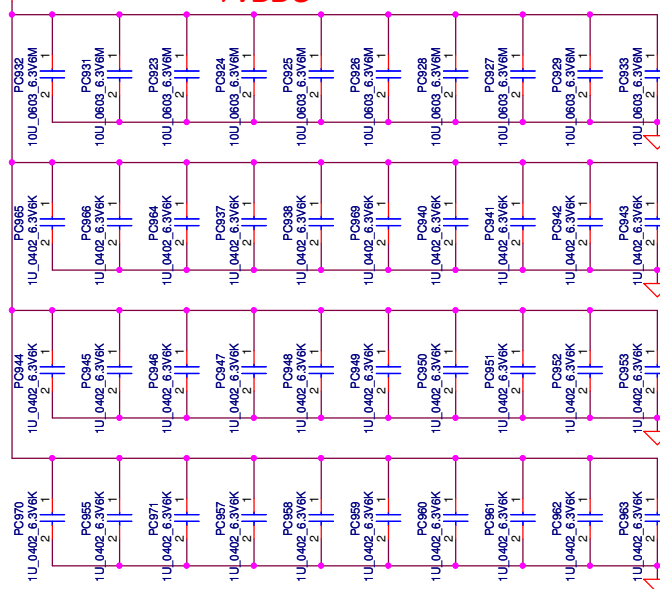
Local



# +VGA\_CORE

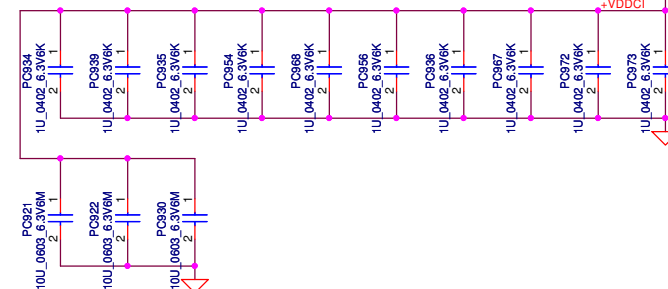
## +VGA\_CORE

## +VDDC



## +VDDCI

## +VDDCI



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